PCN# 20121221001

Fix unstable operation with PLLM at 600 MHz on MityDSP-6711 Family of System On Modules

Date: December 21, 2012
To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Production Manager, Bill Halpin (bill.halpin@criticallink.com).

Sincerely,

Critical Link, LLC
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PCN Number: 20121221001
PCN Date: December 21, 2012
Title: Fix unstable operation with PLLM at 600 MHz
Contact: Bill Halpin
Phone: (315) 425-4045
Ship Date: 12/01/2012

Description of Change

The distribution of the on-board 25 MHz oscillator clock to the FPGA and DSP was changed from what is shown in Figure 1 to that shown in Figure 2.

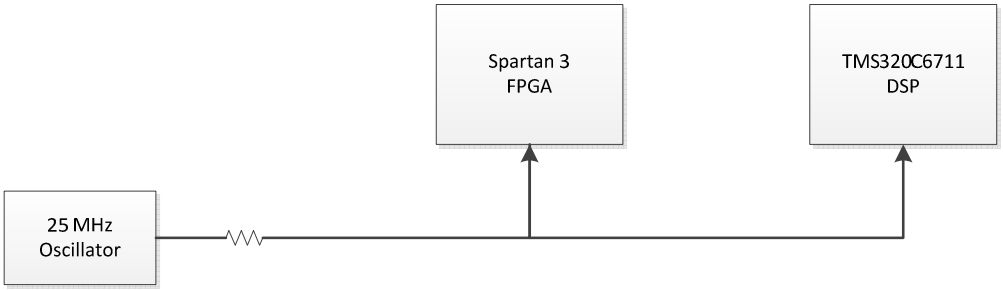

Figure 1 Clock Distribution prior to change

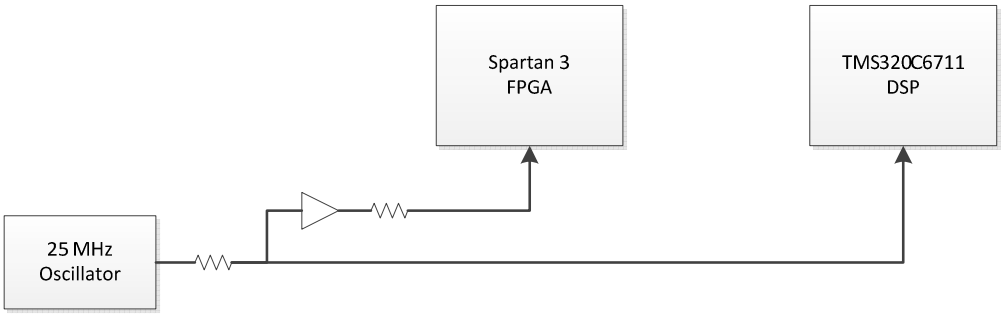

Figure 2 Clock Distribution with change applied

Reason of Change

Recent production runs of MityDSP-6711 and MityDSP-6711 XM processors exhibited instability in the processor phase locked loop circuit. The instability presented as a rapid shift in processor clock frequency (the PLLM output) for approximately 1 to 2 microseconds, long enough to cause the FPGA digital clock manager (DCM) conditioning the EMIFA clock to break lock. This resulted in errors in communication between the DSP and the FPGA on the module.

The root cause of this issue was determined to be a combination of a suboptimal design (the 25 MHz clock source net was bifurcated, feeding both the FPGA and the DSP) and a change in the DSP manufacturing process (the clock input pin

bandwidth increased in sensitivity to as high as 4 GHz) as well as production variances in the FPGA clock input impedance.

By isolating the clock paths as shown in Figure 2, the instability due to reflections in the split clock net was removed.

Work Arounds
Prior to hardware modification, a work around was identified that greatly reduced the occurrence of this issue. The default PLLM setting was 600 MHz. This frequency was divided down to develop the system CPU clock and EMIFA clock. By using a lower PLLM setting such as 400 MHz via a Critical Link provided software function the issue was, in many cases, resolved.

Anticipated Impact on Form, Fit, Function (positive / negative)
No impact on form or fit is anticipated with this change.

Anticipated Impact on Quality or Reliability (positive / negative)
Without this change, some (approximately 20%) of MityDSP-6711 and MityDSP-6711 XM parts manufactured in Q4 2011 and in 2012 could exhibit a momentary loss in communication with the FPGA. Rates in modules exhibiting failures ranged from 1 failure in 5 minutes to 1 failure in several days.

Products Affected:
Details regarding the full printed circuit assembly (PCA) revision history can be located in the MityDSP-6711 Errata on the Critical Link support site.

Model Number	Current PCA	New PCA
6711-KA-1X1-RI	80-000115RI-1E2	80-000115RI-1F
6711-KA-1X1-RC	80-000149RC-1E2	80-000149RC-1F
6711-AA-1X1-RC-L	80-000174RC-1E2	80-000174RC-1F
6711-AB-3X3-RC	80-000157RC-1D2	80-000157RC-1E
6711-AB-3X3-RC-L	80-000163RC-1D	80-000163RC-1E