MitySBC-A5E Single Board Computer (SBC)

Revision History and Errata

17-Mar-2026

1 Introduction

This document describes the production revision history and any known design issues or exceptions to the functional specifications for the MitySBC-A5E Single Board Computer developed by Critical Link, LLC. For the purposes of this document, references to the "SBC" implies MitySBC-A5E Single Board Computer.

Details regarding the board may be accessed at https://www.criticallink.com/product/mitysbc-a5/, and additional support information is located at the following URL: https://support.criticallink.com/redmine/projects/mitysbc_a5/wiki. This document is subject to change without notification. However, the most recent version of this document will be made available at the website mentioned above. The website supports email notification (via the "watch option") for changes to published documents.

2 Product Marking

The board's Printed Circuit Assembly (PCA) number and serial number may be visually read from a label affixed to the top of the board. The Printed Circuit Board (PCB) part number and revision are etched in copper, also visible on the top.

The PCA number begins with "80-". The PCA number can also be determined by the serial number, if necessary. Contact Critical Link for details.

The serial number is an 8 digit number. Generally the first digits are the last two digits of the year manufacture, e.g., boards built in 2026 would have the first two digits in the serial number as 26.

The PCB part number begins with "90-".

3 PCA Product History

The PCA product history for all MitySBC-A5Es is listed in Table 1. Details for Product Change Notifications (PCNs) may be downloaded from the link below. Table 1 highlights the PCA product history for the MitySBC-A5E.

https://support.criticallink.com/redmine/projects/mitysbc_a5/wiki/Errata_and_Product_Change_Notifications

Table 1 Revision History

Model Number*	PCA Number	Applicable Errata / Notes	PCN
A5ED-B96-C7F-RC-SBC-X	80-001679RC-1	Prototype hardware 4.1 Early Silicon Agilex 5 Device 4.2 USB to UART Console Reset Issue 4.3 USB-C Status Lines not Routed to FPGA 4.4 USB-C SuperSpeed TX and RX Lanes are Swapped 4.5 TDK uPol Devices do not Respond on I2C Bus 4.6 Group A / SmartVID Support Not Available 4.7 MIPI Camera 5 not Supported 4.8 Barrel Connector / Smaller Power Supply not Supported 4.9 QSFP+ RX Lanes are in Reverse Order 4.10 Board Serialization not Possible 4.11 Fan Interface not Compatible with COTs Solutions 4.12 Power Dissipation Exceeded for R267 and R273 4.13 Support I3C Pull-ups for Devices with Production Silicon 4.14 Console Serial Lost at Bootup 4.15 PLL Settings for U27 and U29 are not Correct 4.16 I2C_EMAC1 Pull-ups are too Strong 4.17 M.2 M-Key PCIe Connections are not Correct 4.18 M.2 M-Key Slot Mounting Holes are too Large 4.19 FMC I2C Bus Does not Have Pull-up Resistors	

Model Number*	PCA Number	Applicable Errata / Notes	PCN
A5ED-B96-C7F-RC-SBC-X	80-001679RC-2	This is a mod-kit to revision -1 4.1 Early Silicon Agilex 5 Device 4.3 USB-C Status Lines not Routed to FPGA 4.4 USB-C SuperSpeed TX and RX Lanes are Swapped 4.5 TDK uPol Devices do not Respond on I2C Bus 4.6 Group A / SmartVID Support Not Available 4.7 MIPI Camera 5 not Supported 4.8 Barrel Connector / Smaller Power Supply not Supported 4.9 QSFP+ RX Lanes are in Reverse Order 4.10 Board Serialization not Possible 4.11 Fan Interface not Compatible with COTs Solutions 4.12 Power Dissipation Exceeded for R267 and R273 4.13 Support I3C Pull-ups for Devices with Production Silicon 4.14 Console Serial Lost at Bootup 4.15 PLL Settings for U27 and U29 are not Correct 4.16 I2C_EMAC1 Pull-ups are too Strong 4.17 M.2 M-Key PCIe Connections are not Correct 4.18 M.2 M-Key Slot Mounting Holes are too Large 4.19 FMC I2C Bus Does not Have Pull-up Resistors	20260324000
A5ED-B96-C7F-RC-SBC-X A5ED-B96-C7F-RC-SBC A5ED-B96-C7F-RI-SBC A5ED-B94-C7F-RI-SBC	80-001679RC-3 80-001788RC-3 80-001789RI-3 80-001877RI-3	80-001789RI-3 and 80-001877RI-3 should have been designated as “RC”. 4.1 Early Silicon Agilex 5 Device (80-001679RC-5 only) 4.12 Power Dissipation Exceeded for R267 and R273 4.13 Support I3C Pull-ups for Devices with Production Silicon 4.14 Console Serial Lost at Bootup 4.15 PLL Settings for U27 and U29 are not Correct 4.16 I2C_EMAC1 Pull-ups are too Strong 4.17 M.2 M-Key PCIe Connections are not Correct 4.18 M.2 M-Key Slot Mounting Holes are too Large 4.19 FMC I2C Bus Does not Have Pull-up Resistors	20260324001
A5ED-B96-C7F-RC-SBC-X A5ED-B96-C7F-RC-SBC A5ED-B96-C7F-RC-SBC A5ED-B94-C7F-RC-SBC	80-001679RC-4 80-001788RC-4 80-001789RC-4 80-001877RC-4	This is a mod-kit to revision -3 4.1 Early Silicon Agilex 5 Device (80-001679RC-5 only) 4.12 Power Dissipation Exceeded for R267 and R273 4.13 Support I3C Pull-ups for Devices with Production Silicon 4.15 PLL Settings for U27 and U29 are not Correct 4.18 M.2 M-Key Slot Mounting Holes are too Large 4.20 Initial PCIe Root Port Design does not Work with all M.2 NVMe Drives	20260324002

Model Number*	PCA Number	Applicable Errata / Notes	PCN
A5ED-B66-C88-RC-SBC-X A5ED-B66-C88-RC-SBC A5ED-B64-C88-RC-SBC A5ED-B64-C48-RC-SBC A5ED-B64-C44-RC-SBC	80-001679RC-5 80-001789RC-5 80-001877RC-5 80-001897RC-5 80-001898RC-5	4.1 Early Silicon Agilex 5 Device (80-001679RC-5 only) 4.20 Initial PCIe Root Port Design does not Work with all M.2 NVMe Drives	20260324003

* The model number scheme for the MitySBC-A5E was updated to be consistent with the MitySOM-A5E product line. See the datasheet for more details.

4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to MitySBC-A5E single board computers. Please refer to Table 1 to determine which items are applicable to a specific revision of SBC.

4.1 Early Silicon Agilex 5 Device

Issue Description
The Altera Agilex 5 used on the initial MitySBC-A5E board is an Engineering Silicon (ES) device made available by the Altera Early Access Program (EAP). Customers should review related errata documentation from Altera regarding any issues with the Engineering Silicon.

Design Impact
The errata Altera has identified with the ES devices will exist for these initial boards. Please refer to Altera's documentation for further details:
https://docs.altera.com/r/docs/825514/current/agilextm-5-es-device-errata-and-user-guidelines

Planned Resolution
Production devices will be used on future boards.

4.2 USB to UART Console Reset Issue

Issue Description
The USB Console UART chip may not be cleanly reset if a board has been powered down for a period and then is powered up with the USB cable to a host PC installed. When this happens, typically the UART RX LED remains on and the console I/O stops functioning.

Design Impact
Production use for this design should not rely on console communication.

Workarounds
Insert the USB console cable after powering on the device. If your board enters this state, simply unplug and replug the USB cable into the board. This will force a reset.

Planned Resolution
This issue will be corrected in the next version of the hardware (-2 and above).

4.3 USB-C Status Lines not Routed to FPGA

Issue Description
The VBUS detection and fault status lines from the USB-C interface circuitry are not routed to the FPGA properly. In addition, the INT_N from the USB-C port controller is not routed to the FPGA.

Design Impact
This revision of the board will not support dual role operation.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the board will include the necessary connections to support full dual role and USB-C mux / flipping operations.

4.4 USB-C SuperSpeed TX and RX Lanes are Swapped

Issue Description
The transceiver TX and RX lanes assigned for USB-3 SuperSpeed operation on the USB-C port are not connected properly at the TI HD3SS3220IRNHR port controller chip. The TX and RX lanes are swapped.

Design Impact
This revision of the board will not support USB-3 SuperSpeed operation.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the board will swap the TX and RX lanes to the port controller chip to support SuperSpeed data rates.

4.5 TDK uPol Devices do not Respond on I2C Bus

Issue Description
The TDK uPol power supplies used on the SBC to support the 1.1, 1.2, 1.3, 1.8, and 5.0 V supplies were connected to the +1.8V I2C1 bus. They require a minimum of +3.3V I2C levels for proper operation.

Design Impact
The status of the power supplies cannot be read by the HPS. This should not impact the functionality of the board.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the board will put these devices on a level translated I2C bus operating at +3.3V.

4.6 Group A / SmartVID Support Not Available

Issue Description
The current design of the MitySBC does not support Group A devices, or those devices requiring SmartVID control of the core voltage levels.

Design Impact
No design impact on delivered devices, however the configuration will not support installation of Group A (speedgrade –1, -2, -3) devices.

Workarounds
There are no workarounds.

Planned Resolution
Future versions will include a redesigned core power supply utilizing TDK uPol power modules with proper PMBus controls to support Group A SmartVID control.

4.7 MIPI Camera 5 not Supported

Issue Description
MIPI camera 5 shares the same HSIO bank as the HPS LPDDR4 interface. The connections made violate Altera published pin restrictions for the bank.

Design Impact
MIPI camera 5 cannot be used in a design utilizing the HPS LPDDR4.

Workarounds
There are no workarounds.

Planned Resolution
Future versions will have the MIPI camera interface mapped to pins on the HSIO bank that do not violate the Altera pin restrictions.

4.8 Barrel Connector / Smaller Power Supply not Supported

Issue Description
The current design of the SBC utilizes a 4-pin laptop style power connector that is only compatible with a small number of off-the-shelf power supplies. Requests have been made to include support for a more standard barrel style power supply connector.

Design Impact
No design impact.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the MitySBC will include both the 4-pin laptop style connector as well as an optional barrel style power supply connector.

4.9 QSFP+ RX Lanes are in Reverse Order

Issue Description
The QSFP+ RX lane assignments are in reverse order in the layout as compared to the TX lane assignments.

Design Impact
This may create problems with certain protocol implementations, though this topology should be acceptable for 10-40 GB Ethernet solutions.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the PCB will correct the ordering such that both TX and RX channels are in the same order at the connector interface.

4.10 Board Serialization not Possible

Issue Description
No dedicated EEPROM exists on the SBC to store factory configuration, including serial number, assigned MAC address, model number, etc.

Design Impact
There is no software mechanism to identify a specific instance of the SBC being used.

Workarounds
Users must capture the serialization data from the affixed label and store it manually to other media if this feature is needed.

Planned Resolution
Future versions will include a small I2C EEPROM to support storing of factory configuration data.

4.11 Fan Interface not Compatible with COTs Solutions

Issue Description
The mounting holes for the fan are currently only compatible with a custom fan / heatsink solution recommended by the Altera development team during the early access program. The fan / heatsink is not readily available and is overdesigned for the heat dissipation required for most designs.

Design Impact
There is no design impact, but part availability may impact delivery schedule if the issue is not addressed.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the board will include an alternate hole pattern that will support more readily available heatsink and fan solutions.

4.12 Power Dissipation Exceeded for R267 and R273

Issue Description
R267 and R273 on the SBC are current limiting resistors for the +12V power and power good LEDs. The current draw through these resistors is such that the power dissipation exceeds the rating of the part.

Design Impact
The life of the resistors and the LED functionality may be reduced.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the design will replace the resistors with a part that supports the needed power dissipation.

4.13 Support I3C Pull-ups for Devices with Production Silicon

Issue Description
The production silicon version of the Agilex 5 includes a new functional pin to enable board level pull-ups for I3C busses to provide full compliance to the I3C specification. For the I3C0 expansion interface on J19, no pull-ups or control is included in the current design.

Design Impact
Full I3C compliance is not achievable on the I3C0 / J19 expansion interface.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the SBC will include control and pull-ups for the I3C0 expansion interface signals.

4.14 Console Serial Lost at Bootup

Issue Description
During initial boot, the first few characters of the boot sequence output on the console port may be lost.

Design Impact
Customers should not rely on the first line of text output by the boot loader onto the console port for any sort of scripting or board health monitoring.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the SBC will include needed pull-ups in the design to ensure no data is lost during boot up intervals.

4.15 PLL Settings for U27 and U29 are not Correct

Issue Description
The PLL settings for the various clock inputs to the Agilex 5 are not ideal:

- U27-CLK0 (QSFP reference clock) is configured as 1.8V LVDS instead of HCSL output format.
- U27-CLK1 (USB3 reference clock) is configured as 1.8V LVDS instead of HCSL output format.
- U27-CLK2 (DisplayPort reference clock) is configured as 1.8V LVDS instead of HCSL output format.
- U27-CLK3 (SGMII reference clock) is disabled.
- U29-CLK2 (MIPI reference clock 1) is disabled.

Design Impact
While not characterized, U27-CLK0, U27-CLK1, and U27-CLK2 may exhibit additional noise or jitter when configured as LVDS instead of HCSL. Without U27-CLK3 enabled as 125 MHz HCSL, supporting both the SGMII interface (requiring 125 MHz reference clock) as well as the USB-3 interface (requiring a 100 MHz reference clock) is not possible. Without U29-CLK2 enabled as 20 MHz 1.8V LVDS, supporting CAM 5 is not possible.

Workarounds
It is possible, via I2C command script, to enable / reconfigure the clocks after power on. Contact Critical Link for support if needed.

Planned Resolution
Future versions of the SBC will update the clocks per the problem description above.

4.16 I2C_EMAC1 Pull-ups are too Strong

Issue Description
The pull-up resistors on the I2C_EMAC1 bus, used to interface to several devices including the USB-C multiplexer chip and the PLL devices, are too strong.

Design Impact
Accessing the I2C port on the USB-C multiplexer chip is not successful with the current values. This results in the USB-C role switching not working.

Workarounds
There are no workarounds.

Planned Resolution
Future versions will utilize pull-up values that will provide reliable communication with the USB-C multiplexer device.

4.17 M.2 M-Key PCIe Connections are not Correct

Issue Description
The PCIe RX and TX GTS transceiver lanes are not routed in the same order to the PCIe interface pins on the M.2 M-Key connector. RX is ordered 0 -> 3, while TX is ordered 3 -> 0. In addition, the PCIE_PERST connection to the FPGA is not on the required dedicated PCIE1_PERST pin of the Agilex 5.

Design Impact
The M.2 PCIE interface will not function correctly and is not usable.

Workarounds
There are no workarounds.

Planned Resolution
Future versions of the SBC will correct the lane ordering on the transceiver lanes and will route the PCIE_PERST signal to the correct Agilex 5 pin.

4.18 M.2 M-Key Slot Mounting Holes are too Large

Issue Description
The three mounting holes intended to mate with the SM3ZS067U410-NUT1 standoff are too large.

Design Impact
Using the mounting holes with the proper standoff can be done, but the fit will be loose on the board and could require additional washers to ensure the standoff is properly secured to the board.

Workarounds
Using a washer with a pan-head screw will allow the standoff to be secured.

Planned Resolution
Future versions of the SBC will reduce the hole size to be consistent with the SM3ZS067U410-NUT1 specification.

4.19 FMC I2C Bus Does not Have Pull-up Resistors

Issue Description
The FMC I2C bus does not include pull-up resistors on the board to +3.3V, required for proper I2C operation.

Design Impact
It may not be possible to read the FMC identification EEPROM on an installed FMC card.

Workarounds
With some FMC cards, success has been reported utilizing the internal weak pull-up resistor on the HVIO lines of the Agilex 5 connections.

Planned Resolution
Future versions of the SBC will include 4.7k pull-up resistors on this bus.

4.20 Initial PCIe Root Port Design does not Work with all M.2 NVMe Drives

Issue Description
Critical Link has identified some M.2 NVMe PCIe Gen 3 SSDs that do not operate correctly in the M.2 M-Key slot.

Design Impact
Customers intending to use a local NVMe drive for storage may not be able to interface to the drive in a reliable manner if they select an unsupported / untested drive.

Workarounds
Contact Critical Link for a list of SSD drives known to work with the current design.

Planned Resolution
The root cause of this issue has not yet been determined. If a hardware modification is required, future versions of the SBC will include the correction.

5 Revision History

Date	Version	Change Description
17-Mar-2026	1.0	Initial Release