PCN# 20260324001

General Updates from Revision -2 to -3 for

MitySBC-A5E
All Variants

Date: March 24, 2026

To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact us at info@criticallink.com

Sincerely,

Critical Link, LLC

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PCN Number: 20260324001
PCN Date: March 24, 2026
Title: General Updates from Revision -2 to -3
Contact: info@criticallink.com
Phone: (315) 425-4045
Ship Date: Starting Sep 2024

Overview

Changes to MitySBC-A5E are identified in the following sections.

1 Route USB-C Status Lines to FPGA

1.1 Description of Change

The USB-C multiplexer chip INT_N signal was connected to PIN A39 (HVIO_6D_17) of the Agilex-5. The USB-C VBUS was connected via an inverting transistor to pin D34 (HVIO_6D_19) of the Agilex-5. The VBUS power enable control was changed from using the CPEN signal of the USB 2.0 ULPI chip to pin B35 (HVIO_6D_18) of the Agilex-5. All three of the Agilex-5 pins mentioned were previously not connected to anything.

1.2 Reason for Change

These modifications were done in order to properly integrate the USB-C multiplexer control with the Altera provided USB 3.0 IP blocks available in the HPS subsystem.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The modifications allow using the USB-3 superspeed signals and multiplexer chip for the USB-C interface when plugged in either orientation.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

The changes do not affect quality or reliability of the board.

2 Correct USB-C Mux Power Supply Sequencing

2.1 Description of Change

A sequencing circuit was added to ensure that the VCC33 pin of the HD3SS3220IRNHR USB-C multiplexer chip is powered after the VDD5 pin of the HD3SS3220IRNHR chip.

2.2 Reason for Change

The change ensures that the power rail sequencing of the part is consistent with the HD3SS3220IRNHR datasheet.

2.3 Anticipated Impact on Form, Fit, Function (positive / negative)

No expected change to form, fit, or function.

2.4 Anticipated Impact on Quality or Reliability (positive / negative)

It is expected that powering the HD3SS3220IRNHR device according to manufacturer specifications will extend the life of the device. However, Critical Link cannot quantify the change in the expected reliability of the board.

3 Correct I2C level for TDK Voltage Regulators

3.1 Description of Change

The TDK Voltage Regulators (all FS1406 variants) for the 1.1V, 1.2V, and 1.3V supplies, the TDK Voltage Regulators (all FS1412 variants) for the 1.0V and 1.8V supplies, and the TDK Voltage Regulator (FS1403 variant) for the +5.0V supply were connected to a +3.3V level translated version of the HPS I2C_EMAC1 I2C bus controller.

3.2 Reason for Change

The I2C_EMAC1 bus operates at 1.8V. The mentioned supplies from TDK default to requiring +3.3V on the I2C control interface. They do not operate correctly at 1.8V.

3.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The change allows users to interrogate the mentioned supplies using the I2C_EMAC1 data bus. In general, control over the devices is not required, but may be helpful for board level troubleshooting.

3.4 Anticipated Impact on Quality or Reliability (positive / negative)

No impact on quality or reliability is expected.

4 Update Core Power Supplies to support Group A Agilex 5 Devices

4.1 Description of Change

The Agilex-5 Core power supply design, utilizing the TI TPS40428RHAR switching power supply, was redesigned to use a dual stacked TDK FS1525-0600 set of switching power supplies.

4.2 Reason for Change

To support future variants of MitySBC-A5E that include Group A speed grade Agilex 5 parts, the core power supply must support SmartVID control to dynamically change the core supply voltage based on system load and utilization. The existing design did not support SmartVID with the Agilex 5.

4.3 Anticipated Impact on Form, Fit, Function (positive / negative)

No anticipated impact on form, fit, or function is expected with existing variants. Support for faster speed grade Agilex 5 devices is added.

4.4 Anticipated Impact on Quality or Reliability (positive / negative)

No change to quality or reliability.

5 Reroute MIPI camera 5 to honor Altera HSIO Pin Restrictions

5.1 Description of Change

The CAM5 MIPI connections were changed between J8 and the Agilex 5 according to the table below:

J8 Pin	Net Name	-1/-2 “old” connection	-3 “new” connection
N/A	MIPI_REFCLK1_N	Y84	T98
N/A	MIPI_REFCLK2_N	Y87	V98
9	CAM5_CSI_RX3_N	M84	Y95
8	CAM5_CSI_RX3_P	K84	Y98
12	CAM5_CSI_RX2_N	T87	AC86
11	CAM5_CSI_RX2_P	V87	AC90
15	CAM5_CSI_RXCLK_N	M95	AG93
14	CAM5_CSI_RXCLK_P	K95	AG90
18	CAM5_CSI_RX1_N	T95	AC96
17	CAM5_CSI_RX1_P	P95	AC100
21	CAM5_CSI_RX0_N	T98	AG104
20	CAM5_CSI_RX0_P	V98	AG100
N/A	240 Ohm Termination	N/A	P95

5.2 Reason for Change

The CAM5 MIPI signals shared the same HSIO bank as the HPS LPDDR4. The MIPI signal connections previously violated Agilex 5 pin restrictions for the HSIO when sharing a bank with an HPS EMIF controller. The new connections are supported by the device.

5.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change will allow using the CAM5 MIPI camera simultaneously with the HPS LPDDR4 EMIF bank.

5.4 Anticipated Impact on Quality or Reliability (positive / negative)

No change to quality or reliability.

6 Provide Optional Barrel Connector for Main Power Supply

6.1 Description of Change

A 2.1 x 5.5mm barrel connector jack, P1, 694106301002, was added to use as an alternate input to the main +12V input on J17. Users can use either P1 or J17 to power the board.

6.2 Reason for Change

The barrel connector allows use of several off-the-shelf supplies that may be more readily available.

6.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The form was impacted to provide space for the barrel connector. See the mechanical drawings on the Critical Link MitySBC Support Site for more information.

6.4 Anticipated Impact on Quality or Reliability (positive / negative)

No impact on quality or reliability.

7 Reverse QSFP+ Rx Lane order to Agilex 5 FPGA

7.1 Description of Change

The following connection changes were made between the QSFP+ connector and the Agilex 5 FPGA. This change essentially reverses the RX lane order to the GTSL1A_RX channels on the Agilex 5.

J6 Pin	Net Name	-1/-2 "Old" connection	-3 "New Connection"
B25	QSFP_RX3_P	BV135	BF135
B24	QSFP_RX3_N	BV133	BF133
A14	QSFP_RX2_P	BN135	BJ135
A15	QSFP_RX2_N	BN133	BJ133
B22	QSFP_RX1_P	BJ135	BN135
B21	QSFP_RX1_N	BJ133	BN133
A17	QSFP_RX0_P	BF135	BV135
A18	QSFP_RX0_N	BF133	BV133

7.2 Reason for Change

This change was made to make the ordering of the Rx channels and Tx channels be consistent at the interface to the Agilex 5, a recommended practice by Altera.

7.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The pin mapping should be supported for 40 Gbe in either configuration due to protocol channel mapping, however the Altera Quartus Pro tool requires the Tx/Rx lanes to be mapped in the same order to properly place and fit a design utilizing the GTS IP.

7.4 Anticipated Impact on Quality or Reliability (positive / negative)

No change in Quality or Reliability.

8 Add I2C EEPROM for Board Serialization Data

8.1 Description of Change

An I2C EEPROM, CAT24C256WI, was added to the I2C_EMAC1 I2C bus at address 0x50.

8.2 Reason for Change

Field support for Critical Link products often requires the serial number of the board to track the unit to a specific build and artifacts collected during factory test. Customers may not always be able to visually collect this information in fielded systems. Often if there is a software mechanism to collect this information this challenge can be overcome.

8.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The change will allow saving and retrieving board specific information (e.g., serial number, model number, assigned MAC address) via I2C from the HPS during operation.

8.4 Anticipated Impact on Quality or Reliability (positive / negative)

No expected impact on quality or reliability is expected.

9 Add mCONFIG push button, S3

9.1 Description of Change

A normally open, momentary contact, push button to ground (S3) was added to the Agilex 5 nCONFIG pin.

9.2 Reason for Change

This is an added feature to allow users to force an FPGA / SDM reconfiguration without power cycling the board or utilizing the JTAG interface.

9.3 Anticipated Impact on Form, Fit, Function (positive / negative)

An additional push button, S3, will be present on the board allowing manual FPGA / SDM reconfiguration.

9.4 Anticipated Impact on Quality or Reliability (positive / negative)

No expected impact on quality or reliability.

10 Add DEBUG1 and DEBUG2 LEDs

10.1 Description of Change

Two green LEDS, D21 (DEBUG1) and D22 (DEBUG2), were added to the board design. They are controlled with active high outputs on HVIO_6B_17 (ball CK2) and HVIO_6B_18 (ball CJ2), respectively.

10.2 Reason for Change

This is an added feature to allow users access to LEDs for debugging or application specific functions.

10.3 Anticipated Impact on Form, Fit, Function (positive / negative)

An additional set of LEDs will be present on the board, however the overall form, fit, and function has not changed.

10.4 Anticipated Impact on Quality or Reliability (positive / negative)

No expected impact on quality or reliability.

11 Update Mechanical Mounting holes for Agilex 5 heatsinks

11.1 Description of Change

The through hole mounting holes intended for the Agilex 5 heatsink and fan were changed from Figure 1 to Figure 2.

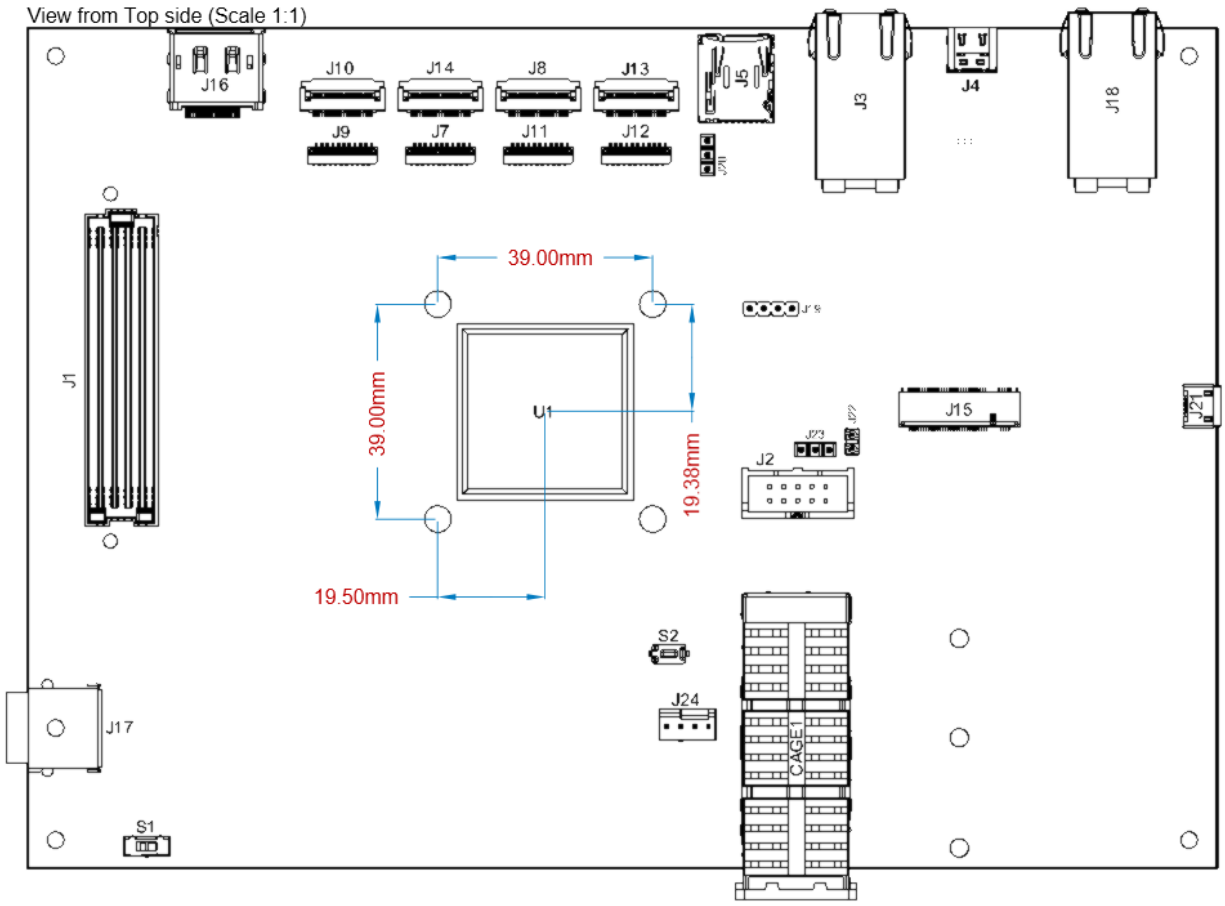

Figure 1 -1/-2 "Old" Heatsink Mounting Hole Dimensions

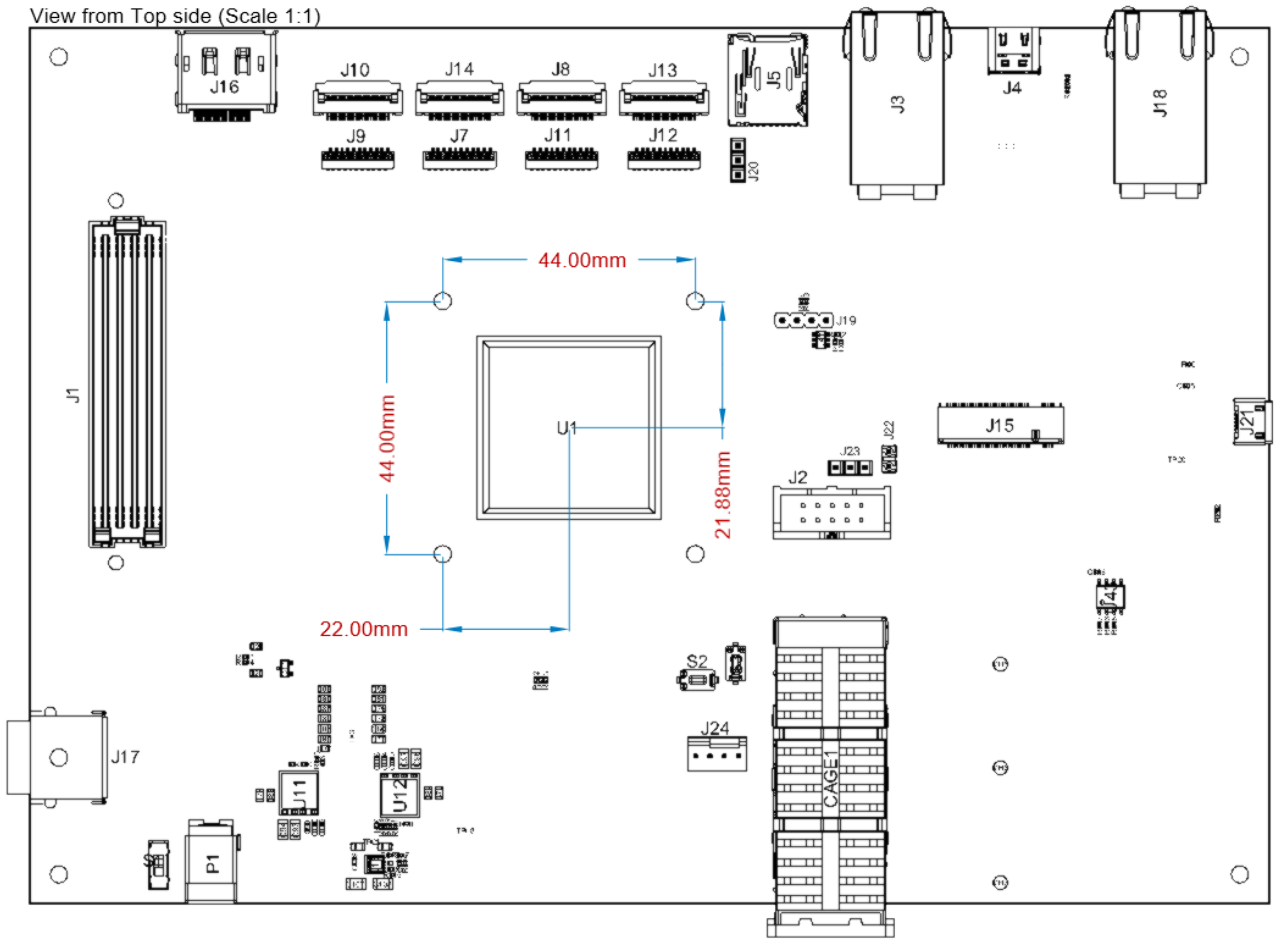

Figure 2 -3 "New" Heatsink Mounting Hole Dimensions

11.2 Reason for Change

The original mounting holes were designed for a customer heatsink, Heatscape HTSP-ASM-INT1-134-06-01, recommended by Altera. This heatsink and fan arrangement is not widely available, and prohibitively expensive.

The updated mounting holes allow for more widely available heatsinks, including the Advanced Thermal Solutions ATS-61500K-C2-R0.

11.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The form factor was updated to support the new mounting hole pattern.

11.4 Anticipated Impact on Quality or Reliability (positive / negative)

No expected impact on quality or reliability.

12 Swap USB-C Superspeed TX and RX Lanes to Port Controller

12.1 Description of Change

The following connection changes were made between the Agilex 5 FPGA transceiver ports and the USB-C port controller chip, HD3SS3220IRNHR.

FPGA Connection	Net Name	-1/-2 “Old” Port Controller connection	-3 “New” Port Controller Connection
B25	USB1_SSRX_N	Pin 9	Pin 6
B24	USB1_SSRX_P	Pin 10	Pin 7
A14	USB1_SSTX_N	Pin 6	Pin 9
A15	USB1_SSTX_P	Pin 7	Pin 10

12.2 Reason for Change

This change was needed to allow the port controller chip to properly pass the TX and RX superspeed signals correctly to the USB-C connector.

12.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change allows the superspeed / USB-3 signals to work correctly with devices plugged into the USB-C port. There is no impact on form or fit.

12.4 Anticipated Impact on Quality or Reliability (positive / negative)

No change in Quality or Reliability.

13 Products Affected

Details regarding the full revision history are in the MitySBC-A5E Revision History section on the Critical Link support site.

https://support.criticallink.com/redmine/projects/mitysbc_a5/wiki/Errata_and_Product_Change_Notifications

Model Number	Starting PCA	Replacement PCA
A5ED-B96-C7F-RC-SBC-X	80-001679RC-2	80-001679RC-3
A5ED-B96-C7F-RC-SBC	N/A	80-001788RC-3
A5ED-B96-C7F-RI-SBC	N/A	80-001789RI-3
A5ED-B94-C7F-RI-SBC	N/A	80-001877RI-3

Table 1: Products Affected

14 Document Revision History

Date	Version	Change Description
24-March-2026	1.0	Initial Version