PCN# 20260324003

Updates from revision -4 to -5 for

MitySBC-A5E
All Variants

Date: March 24, 2026

To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the info@criticallink.com

Sincerely,

Critical Link, LLC

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PCN Number: 20260324002
PCN Date: March 24, 2026
Title: Updates from revision -4 to -5
Contact: info@criticallink.com
Phone: (315) 425-4045
Ship Date: Starting Feb 2026

Overview

Changes to MitySBC-A5E are identified in the following sections.

1 Replace current limiting resistors for +12V Power and Power Good LED

1.1 Description of Change

R267 and R273 were replaced with resistors of similar value but higher power rating.

1.2 Reason for Change

R267 and R273 are current limiting resistors for the +12V Power and Power Good LEDs on the board. The previous design utilized a part whose power dissipation was rated lower than the power dissipated by the resistors when the LEDs where enabled.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

No change to form, fit, or function is expected.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

It is expected that the overall lifetime of the R267 and R273 will be extended by operating the devices within their rated power dissipation specifications.

2 Install R298 and R322

2.1 Description of Change

A 4.87K ohm resistor (R298) was installed between the U12 ADDR pin (12) and ground. A 4.7K pullup resistor was installed on the SMB_PMBCLK net, attached to the SCL nets of U12 and U11.

2.2 Reason for Change

The change is needed to support correct I2C address resolution of U12 and facilitate I2C communications to the TDK core power supplies.

2.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The change allows I2C communication with the TDK voltage regulators supplying the Agilex 5 core power supply. The devices will operate without I2C communication, however for SmartVID variants, the I2C / PMBUS communication is required.

2.4 Anticipated Impact on Quality or Reliability (positive / negative)

No impact to quality or reliability is expected with this change.

3 Replace EOL and Obsolete Parts

3.1 Description of Change

The parts listed in the table below were replaced due to obsolescence / availability issues.

Designator	Old Part Number	New Part Number
L2	IHLP1212BZER1R0M11	IHLP1212BZEZ1R0M1Z
L3	IHLP1212BZER1R0M11	IHLP1212BZEZ1R0M1Z
L4	IHLP1212BZER1R0M11	IHLP1212BZEZ1R0M1Z
U30	74AXP1T34GWH	SN74LXC1T14DCKR
U26	MTFC64FAZAQHD	MTFC64GBCAQTC-AITC

3.2 Reason for Change

The noted parts are obsolete.

3.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There are no expected changes to form, fit, or function.

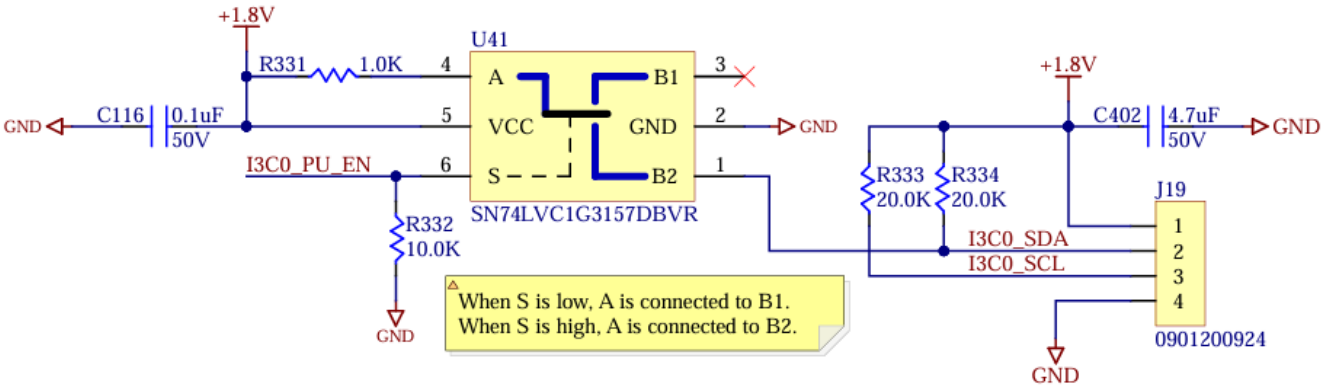
3.4 Anticipated Impact on Quality or Reliability (positive / negative)

No impact on quality or reliability is expected.

4 Connect I3C Pullup enable pin and pullup circuit for I3C0 signals.

4.1 Description of Change

The circuitry shown below was added to the I3C0 bus on the J19 expansion connector. The I3C0_PU_EN net is tied F127 of the Agilex 5 FPGA. The ETH1_RESETN net, previously connected to F127 of the Agilex 5 FPGA, has been moved to pin T132 of the FPGA (GPIO0_IO11), previously not used.



4.2 Reason for Change

To fully support the I3C standard, Altera requires the above circuitry to enable the pullups on the I3C bus when required.

4.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change allows compliance to the I3C bus on the J19 connector. Customers using the ETH1_RESETN line will need to update their firmware to use the newly assigned pin.

4.4 Anticipated Impact on Quality or Reliability (positive / negative)

No change to quality or reliability is expected.

5 Default pre-programmed PLL settings updated

5.1 Description of Change

The default, pre-programmed settings for U27 and U29 (PLL devices) have been updated according to the table below.

PLL Designator	CLK Number	Frequency		Format		Destination
		Old	New	Old	New	
U27	CLK0	156.25 MHz	156.25 MHz	1.8V LVDS	HCSL	QSFP+ RefClk
U27	CLK1	100 MHz	100 MHz	1.8V LVDS	HCSL	USB 3 RefClk
U27	CLK2	150 MHz	150 MHz	1.8V LVDS	HCSL	DisplayPort Refclk
U27	CLK3	N/A	125 MHz	Disabled	HCSL	GXB Spare Refclk
U29	CLK0	100 MHz	100 MHz	1.8 LVDS	1.8 LVDS	HPS LPDDR4 EMIF Refclk
U29	CLK1	100 MHz	100 MHz	1.8 LVDS	1.8 LVDS	FPGA LPDDR4 EMIF Refclk
U29	CLK2	N/A	20 MHz	Disabled	1.8V LVDS	MIPI Bank 3A Refclk
U29	CLK3	20 MHz	20 MHz	1.8 LVDS	1.8 LVDS	MIPI Bank 3B Refclk

5.2 Reason for Change

While the parameters for the Si5338 PLL 1.8V LVDS output (when A/C coupled) meet the differential input requirements for the clocks connected to the Agilex 5 Transceiver reference clocks, Altera recommends that either HCSL or CML standard be used. U27 CLK3 was enabled at 125 MHz to support the SGMII transceiver interface. U29 CLK2 was enabled to support the CAM5 MIPI camera interface. The PLL clocks can be modified via the Agilex 5 HPS via the I2C bus. See the Critical Link MitySBC-A5E support site for more details.

5.3 Anticipated Impact on Form, Fit, Function (positive / negative)

No impact to form, fit, or function is expected.

5.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no impact on quality or Reliability with this change.

6 Reduce m.2 M-Key Mounting hole diameters

6.1 Description of Change

The size of the 3 mounting holes used to install a standoff for attaching an m.2 M-key card was updated to be consistent with the JAMECO SM3ZS067U410-NUT1 standoff part. This part is recommended for use with the J15 connector.

6.2 Reason for Change

The mounting holes are tool large for the recommended standoff. This can cause installation and alignment problems when fitting an m.2 NVME card onto the board.

6.3 Anticipated Impact on Form, Fit, Function (positive / negative)

The form factor is such that it should be easier to install an m.2 NVME card into the system.

6.4 Anticipated Impact on Quality or Reliability (positive / negative)

No impact on quality or reliability is anticipated with this change.

7 Model Numbering Scheme Updated

7.1 Description of Change

The model number on the PCA label of the board has been updated according to the most recent version of the MitySBC standard.

7.2 Reason for Change

To be more consistent with the MitySOM-A5E Agilex 5 family of devices, the model number scheme was updated to use common codes for speed grade, FPGA density, RAM and eMMC size.

7.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no impact on form, fit, or function.

7.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no impact on reliability or quality.

8 Products Affected

Details regarding the full revision history is in the MitySBC-A5E Revision History section on the Critical Link support site.

https://support.criticallink.com/redmine/projects/mitysbc_a5/wiki/Errata_and_Product_Change_Notifications

Model Number	Starting PCA	Replacement PCA
A5ED-B66-C88-RC-SBC-X	80-001679RC-4	80-001679RC-5
A5ED-B66-C88-RC-SBC	80-001788RC-4	80-001788RC-5
A5ED-B64-C88-RC-SBC	80-001789RC-4	80-001789RC-5
A5ED-B64-C88-RC-SBC	80-001877RC-4	80-001877RC-5
A5ED-B64-C44-RC-SBC	N/A	80-001898RC-5

Table 1: Products Affected

9 Document Revision History

Date	Version	Change Description
24-March-2026	1.0	Initial Version