PCN# 20260608000

Software Update: PMIC I2C address change 0x41 -> 0x40

Date: June 8, 2026

To: Purchasing Agents & Design Engineers

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Hardware Manager Alex Block.

Sincerely,

Critical Link, LLC

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Contact: Alex Block

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EOL Date: June-2025, Rev -3 variants only

Overview

Changes to MitySOM-AM62A System on Modules are identified in the following sections. These changes should only affect early adopters of the module.

1 Change Default

1.1 Description of Change

The revision -3 and earlier variants of the MitySOM-AM62A provide a default 0.75V VDD_CORE Voltage from an on-board power management integrated circuit (PMIC) device, TPS62871QWRXSRQ1 (I2C address 0x41). Revision -4 devices will provide a default 0.85V power rail to supply the VDD_CORE voltage to the AM62A processor device by utilizing a TPS62872Y4QWRXSRQ1 device (I2C address 0x40).

As a supplement to the physical hardware component changes detailed in PCN#20250509000, this update notes that a software change is required to dynamically handle the I2C address shift between production revisions for the PMIC device.

1.2 Reason for Change

To support the 1.4 GHz ARM Cortex-A53 operating performance point (OPP), the VDD_CORE core voltage must be 0.85V. On the older revisions, Critical Link software was adjusting the VDD_CORE voltage from 0.75V to 0.85V during the boot process prior to enabling the 1.4 GHz OPP. Texas Instruments (TI) has advised Critical Link that dynamically adjusting the VDD_CORE voltage once the boot software has loaded is not officially supported for the AM62A family of devices. If the VDD_CORE voltage is not adjusted, then at 0.75V the MitySOM-AM62A maximum CPU speed should be limited to the 1.250 GHz OPP. Changing to the 0.85V VDD_CORE PMIC will allow enabling the 1.4 GHz OPP in a manner that is officially supported by TI.

Furthermore, because the revision -4 PMIC utilizes a different I2C slave address than previous revisions, Device Tree Blob (DTB) fixups are necessary before booting the Linux Kernel. This allows the software stack to dynamically probe the hardware, locate the active PMIC on the bus, and correctly update the PMIC address at boot time.

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1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

Per PCN#20250509000: Starting at revision 10.0 of Critical Link's SDK release, the VDD_CORE voltage will no longer be adjusted by the boot software. Revision -3 (and earlier) SOMs will be limited to a maximum OPP of 1.25 GHz while newer SOMs will support up to 1.4 GHz. However this didn't take into account the PMIC i2c change.

To maintain full software compatibility across both older and newer SOM hardware revisions, customers must integrate the runtime I2C address fixups present in Critical Link's AM62A supported U-Boot 2025.01. Without this software implementation, users with Revision -4 hardware will fail to properly communicate with the new PMIC device and processor frequency scaling will get disabled. No other impact on Form, Fit, Function is expected.

cea3603b: "mitysom-62a: dts: Update I2C address for TPS62871"

6eb14159: "mitysom-62a: Add pmic_fixup for TPS62871 I2C address change"

This software change was released as part of SDK 11.01.07.05 (20260429). We strongly suggest updating SDK versions for this and other changes, however if you need help backporting this change, please reach our to us.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

Critical Link has not observed any issues with boot or processor stability with the older (-3 and below) revisions of the MitySOM-AM62A when adjusting the VDD_CORE voltage prior to enabling the 1.4 GHz OPP. While there is no known impact to Quality or Reliability, the implementation of the dynamic software fixup ensures seamless backward and forward compatibility between hardware variants. It is anticipated that the change will bring additional design margin to the SOM and improve long term quality of the product.

2 Products Affected

Details regarding the full revision history are located in the MitySOM-AM62A Revision History section on the Critical Link support site.

https://support.criticallink.com/redmine/projects/mitysom_am62x/wiki/Errata_and_Module_Product_Change_Notifications

Table 1 Products Affected

Model Number	Starting PCA	Replacement PCA
62A74-TX-XXD-RI	80-001734RI-3	80-001734RI-4
62A74-TX-X9D-RC	80-001735RC-3	80-001735RC-4
62A74-TX-XAE-RI	80-001736RI-3	80-001736RI-4

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3 Document Revision History

Date	Version	Change Description
6-08-2026	1.0	Initial Version

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