

MitySOM-A5E Mini System-On-Module (SOM)

Revision History and Errata

1 Introduction

This document describes the production revision history and any known design issues or exceptions to the functional specifications for the MitySOM-A5E Mini Module developed by Critical Link, LLC. For the purposes of this document, reference to the “module” implies MitySOM-A5E Mini System-On-Module.

Details regarding the board may be accessed at <https://www.criticallink.com/product/mitysom-a5e/>, and additional support information is located at the following URL: https://support.criticallink.com/redmine/projects/mitysom_a5/wiki. This document is subject to change without notification. However, the most recent version of this document will be made available at the website mentioned above. The website supports email notification (via the “watch option”) for changes to published documents.

2 Product Marking

The board’s PCA number and serial number may be visually read from a label affixed to the bottom of the module. The Printed Circuit Board (PCB) part number and revision is etched in copper, also visible on the bottom.

The PCA number begins with “80-”. The PCA number can also be determined by the serial number, if necessary. Contact Critical Link for details.

The serial number is of the format “S/NXXXXXX”, where XXXXXX is the serial number.

The PCB part number begins with “90-”.

3 PCA Product History

The PCA product history for all MitySOM-A5E Mini SOMs is listed in Table 1. Details for Product Change Notifications (PCNs) may be downloaded from the link below. Table 1 highlights the PCA product history for the MitySOM-A5E Mini module. Items shown with red font and crossed out have been removed from production status (obsolete, or end of life).

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Errata_and_Module_Product_Change_Notifications

Table 1 PCA Product History

Model Number	PCA Number	Errata	PCN
A5ED-B9-XXF-RI-X	80-001748RI-1	4.1.1 Early Silicon Agilex 5 Device 4.2.1 Insertion / Removal Force too high for production modules 4.2.2 No provision for chip attached heat sinks 4.3.1 Intermittent Communication with PMICs on I2C1 4.3.2 Several HVIO Banks are not length matched 4.3.3 Agilex 5 Core Voltage Limited to 25A 4.3.4 GTS Transceiver Signal Integrity Margins Above 17G	
A5ED-B06-1X2-MRI-CS A5ED-B16-1X4-MRI-CS A5ED-B14-1X4-MRC-B0 A5ED-B14-1X8-MRC-B0 A5ED-A43-1X4-MRI A5ED-B44-1X4-MRI	80-001843RI-2 80-001844RI-2 80-001868RC-2 80-001869RC-2 80-001880RI-2B 80-001881RI-2B	4.1.1 Early Silicon Agilex 5 Device 4.3.1 Intermittent Communication with PMICs on I2C1 4.3.2 Several HVIO Banks are not length matched 4.3.3 Agilex 5 Core Voltage Limited to 25A 4.3.4 GTS Transceiver Signal Integrity Margins Above 17G	PCN20240909000
A5ED-B06-1X2-MRC A5ED-B06-1X2-MRI A5ED-B16-1X2-MRC A5ED-B16-1X2-MRI A5ED-B66-1X4-MRC A5ED-B66-1X4-MRI A5ED-B06-1X2-MRI-CS A5ED-B16-1X4-MRI-CS ~~A5ED-B14-1X4-MRC-B0~~ ~~A5ED-B14-1X8-MRC-B0~~ A5ED-A43-1X4-MRI A5ED-B44-1X4-MRI A5ED-B64-1X4-MRC A5ED-B64-1X4-MRI	80-001790RC-3 80-001791RI-3 80-001792RC-3 80-001793RI-3 80-001794RC-3 80-001795RI-3 80-001843RI-3 80-001844RI-3 ~~80-001868RC-3~~ ~~80-001869RC-3~~ 80-001880RI-3 80-001881RI-3 80-001913RC-3 80-001914RI-3		PCN20260924000

4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to MitySOM-A5E Mini module.

4.1 Agilex 5

4.1.1 Early Silicon Agilex 5 Device

Issue Description

The Altera Agilex 5 used on the initial MitySOM-A5E Mini modules is an Early Silicon (ES) device. To easily identify the modules with ES silicon parts, review the model number (e.g., A5ED-B9-XXF-RI-X). Any module with the -X extension includes an ES device.

Design Impact

The errata Altera has identified with the ES devices will exist for these initial modules. Please refer to Altera's documentation for further details:

<https://www.intel.com/content/www/us/en/docs/programmable/825514/current/specific-errata-for-the-es-devices.html>

Planned Resolution

Production devices will be used on future modules. The modules with production parts on them will include 4 mounting holes instead of 2.

4.2 Mechanical Interfaces

4.2.1 Insertion / Removal Force too high for production modules

Issue Description

The initial MitySOM-A5E Mini modules used a 400 contact Samtec LP Array™ series LPAF-50-03.5-L-08-2-K-TR board to board connector. This connector presents too high of an insertion and removal force for typical use.

Design Impact

Care must be used to install a SOM into a new carrier board to ensure that neither the SOM nor Carrier card are damaged due to board flex. External tooling is needed to remove a SOM without the potential of damaging the interface connector.

Planned Resolution

Production SOMs will be provided using a Samtec SEARAY™ series SEAF-50-05.0-S-08-2-A-K-TR connector, which provides a lower insertion force.

This is addressed by PCN 20240909000.

4.2.2 No provision for chip attached heat sinks

Issue Description

The initial MitySOM-A5E Mini modules included components placed very close to the FPGA device on the board. The placement of the parts precluded the use of off the shelf chip attached heat sinks, a desirable option for designs using a relatively low amount of power from the FPGA device.

Design Impact

On the preproduction devices, customers will need to use a custom heat spreading solution or an off-the-shelf heatsink with some sort of thermal epoxy or other bonding agent to attach to the FPGA if thermal management is required.

Planned Resolution

Production SOMs will arrange the components on the board such that there is enough clearance around the FPGA to support use of the Advanced Thermal Solutions (ATS) superGRIP™ Heat Sink Attachment Hardware or similar style attachment devices.

This is addressed by PCN 20240909000.

4.3 Design Issues

4.3.1 Intermittent Communication with PMICs on I2C1

Issue Description

The FS1406 supply regulators on these devices are connected to the I2C1 bus and operate at 3.3V by default, while the I2C1 bus operates at 1.8V. As a result, these devices cannot be read reliably, and their presence on the bus may introduce noise and signal-integrity problems that can affect communication with other devices sharing the bus.

Design Impact

Telemetry and configuration reads from the affected FS1406 supplies are unreliable. In addition, the level mismatch degrades overall I2C1 bus integrity, which may intermittently disrupt communication with other devices on the same bus.

Planned Resolution

The FS1406 supply regulators have been removed from the I2C1 bus. Once removed, the affected supplies are no longer accessible over I2C1 and no longer contribute to bus noise.

Baseboard designers should treat the I2C1 addresses previously assigned to these devices as reserved and must not reuse them for other baseboard peripherals, as these FS1406 devices (or similar) may be re-added to the bus in a future revision. The table below lists the reserved addresses for the SOMs.

Table 2 MitySOM-A5E Mini I2C1 Addresses

Address	Device	Feature
0001100	FS1406	0.8V Power Supply (reserved, not previously available)
0001011	FS1406	1.1V Power Supply
0001010	FS1406	1.0V Power Supply
0001001	FS1406	1.2V Power Supply
0001000	FS1406	1.8V Power Supply

This is addressed by PCN 20260924000.

4.3.2 Several HVIO Banks are not length matched

Issue Description

The signals from HVIO Banks on the Agilex 5 FPGA to the balls of the J1 board to board connector are not length matched.

Design Impact

Customers designing a high speed parallel interface must accommodate for the length mismatch / time skew on their carrier card. If the skews are not accounted for, then the amount of margin in the signal integrity of the bus will be reduced. The carrier design guide also indicates that these signals are length matched within a bank. Details for the signal lengths can be found on the [Critical Link support site](#).

Planned Resolution

Except for HVIO Bank 6B, the board has been updated such that each signal within an HVIO bank is length matched to the other nets in the same bank. The carrier design guide will also be updated to note Bank 6B and the change in revision.

This is addressed by PCN 20260924000.

4.3.3 Agilex 5 Core Voltage Limited to 25A

Issue Description

For FPGA devices having 434 KLE or more logic elements, the initial design of the Agilex-5 core voltage power supply used a dual phase switching regulator design in a master/slave topology to supply up to 50A of current. On some modules, there was a race condition observed between the master and slave startup that would result in

intermittent failure to turn on. To mitigate the failure mode, all units have been reworked to disable the slave device, and the core voltage current has been limited to 25A.

Design Impact

Critical Link has investigated several designs, including developing an FPGA “heater” style design, and has not observed a current demand higher than approximately 15A in the worst case 656 KLE scenario. More typical applications consume approximately 10A. The 25A design point still provides an additional 10A of margin for unforeseen FPGA configurations. For most practical designs, there should be no impact with this change. Customers with designs requiring more than 25A of core voltage current should contact Critical Link for a higher current solution.

Planned Resolution

The maximum available current for all FPGA devices will be limited to 25A. This will be reflected in the datasheet and carrier design guides.

This is addressed by PCN 20260924000.

4.3.4 GTS Transceiver Signal Integrity Margins Above 17G

Issue Description

For GTS Transceiver operation above 17G, the insertion loss and return loss characteristics of the module layout are not optimized.

Design Impact

Customers intending to use Group A Agilex 5 device silicon operating at rates up to 28G may have reduced signal integrity margin when integrating the SOM with a carrier card design.

Planned Resolution

The layout of the transceiver lanes on the SOM has been improved (better anti-pad topology, proper return vias, etc.) such that a carrier board design can support the high frequency protocols provided by Agilex 5 Group A devices.

This is addressed by PCN 20260924000.

5 REVISION HISTORY

Date	Version	Change Description
09-September-2024	1.0	Initial Version
24-September-2026	1.1	Update to use MitySOM-A5E Mini name. Add sections 4.3, 4.3.1, 4.3.2, 4.3.3 and 4.3.4. Updated Table 1 to include revision -3 information.