

PCN# 20260924000

Match lengths on HVIO Bank groups, remove FS1406 Supply Regulators from I2C1 bus, limit the FPGA core supply to single-phase (25A) operation, and improve GTS signal integrity margins on the

MitySOM-A5E Mini
Agilex 5 Modules

Date: September 24, 2026

To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact info@criticallink.com

Sincerely,

Critical Link, LLC

Phone: (315) 425-4045

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Phone: (315) 425-4045

Ship Date: Starting March 2027

Overview

Changes to MitySOM-A5E Mini are identified in the following sections.

1 Match Routing Lengths of HVIO Banks

1.1 Description of Change

The signal trace lengths between the Agilex 5E FPGA and the J1 connector interface for HVIO Banks 5A, 5B, 6A, 6C, and 6D have been updated such that signals within the same bank are matched in length to within ± 5 mils. Note that Bank 6B could not be matched.

1.2 Reason for Change

Customers designing a high speed parallel interface utilizing HVIO bank signals had to be aware of the SOM level skews or would suffer reduced margin on the bus signal integrity due to skew mismatch. Matching the lengths as much as possible reduces the risk of introducing skew on an overall design and is consistent with the guidelines in the MitySOM-A5E Carrier Design Guide. Additional information about SOM level skews can be found on the [Critical Link support site](#).

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change should not affect form or fit. This change affects SOM level skew / delays on HVIO lanes. Customers migrating from a -2 revision board to a -3 revision board should review the overall skew (including that introduced by the carrier) and adjust their design if it is warranted.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

None.

2 Removal of FS1406 Supply Regulators from the I2C Bus

2.1 Description of Change

The local FS1406 supply regulators, supporting 0.8V, 1.1V, 1.2V, 1.0V, and 1.8V, have been removed from the I2C bus.

2.2 Reason for Change

The FS1406 devices connected to the I2C1 bus operate at a default I/O voltage level (3.3V) that does not match the I2C1 bus driver (1.8V). As a result, they cannot be read reliably, and their presence may introduce noise and

signal-integrity problems that can disrupt communication with other devices on the bus. Interaction with these devices is not required for proper device operation.

2.3 Anticipated Impact on Form, Fit, Function

There is no impact to form or fit. The FS1406 supplies are no longer accessible over the I2C bus. The I2C addresses previously assigned to these devices remain reserved and must not be reused by the baseboard for other peripherals, as these devices may be re-added to the bus in a future revision. Reserved addresses are listed in the table below:

Table 1 MitySOM-A5E Mini I2C1 Addresses

Address	Device	Feature
0001100	FS1406	0.8V Power Supply (reserved, not previously available)
0001011	FS1406	1.1V Power Supply
0001010	FS1406	1.0V Power Supply
0001001	FS1406	1.2V Power Supply
0001000	FS1406	1.8V Power Supply

2.4 Anticipated Impact on Quality or Reliability

Removing these devices increases the reliability of I2C communications on the I2C1 bus. There is no adverse impact to quality.

3 Core Supply Operated in Single-Phase Mode (25A Limit)

3.1 Description of Change

The FPGA core rail (VCC_CORE) is generated by a TDK FS1525 dual-phase regulator. Starting at revision -2 of the SOM, the slave phase of this regulator has been disabled, and the core supply now operates from the master phase alone, limiting the core rail to 25A. Starting at revision -3 of the SOM, the slave regulator device is not populated on the device. This change applies only to MitySOM-A5E Mini SOMs that include a 434 KLE or higher density FPGA. Devices with less than 434 KLE density are not affected.

3.2 Reason for Change

With both phases enabled, one of the two phases occasionally failed to enable during power-on, resulting in a latched-off fault state and an intermittent power-on (PON) failure. No power-on issues have been observed with the core supply operating from the master phase alone.

3.3 Anticipated Impact on Form, Fit, Function

There is no impact to form or fit. The maximum available FPGA core supply current is limited to 25A. Critical Link has performed extensive validation of this configuration, including maximum-power “heater” core designs intended to maximize core current draw, and has not found a case in which the 25A single-phase supply was insufficient.

Because 25A is below the theoretical maximum core supply demand for these devices, customers should verify their design’s core power requirement using the Intel Quartus Prime Power Estimation tool to confirm that it

remains within the 25A limit. If the estimate exceeds 25A, customers should contact Critical Link, as a higher current option may be available.

3.4 Anticipated Impact on Quality or Reliability

Operating the core supply from a single phase eliminates the intermittent power-on failure and improves power-up reliability. There is no adverse impact to quality.

4 Improve Signal Integrity Margins on GTS Transceiver Signals

4.1 Description of Change

The trace layout of the GTS transceivers between the Agilex 5 FPGA and the J1 connector interface has been optimized to improve signal integrity margins for signals operating above 17G. This has been accomplished by refining the signal via anti-pads and ground return vias.

4.2 Reason for Change

To support carrier card designs targeting GTS transceiver rates supported by Agilex 5E Group A devices (between 17G and 28G), the SOM trace routing has been enhanced to provide improved signal integrity margins at these rates.

4.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change should not affect form or fit. With this change, carrier card designs benefit from improved GTS signal integrity margins above 17G (device Group A speeds).

4.4 Anticipated Impact on Quality or Reliability (positive / negative)

None.

5 Products Affected

Details regarding the full revision history are in the MitySOM-A5E Mini Revision History and Errata on the Critical Link support site at the link below.

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Errata_and_Module_Product_Change_Notifications

Table 2 Products Affected

Model Number	Starting PCA	Replacement PCA
A5ED-B06-1X2-MRC	80-001790RC-2	80-001790RC-3
A5ED-B06-1X2-MRI	80-001791RC-2	80-001791RC-3
A5ED-B16-1X2-MRC	80-001792RC-2	80-001792RC-3
A5ED-B16-1X2-MRI	80-001793RI-2	80-001793RI-3
A5ED-B66-1X4-MRC	80-001794RC-2	80-001794RC-3
A5ED-B66-1X4-MRI	80-001795RI-2	80-001795RI-3
A5ED-B06-1X2-MRI-CS	80-001843RI-2	80-001843RI-3
A5ED-B16-1X4-MRI-CS	80-001844RI-2	80-001844RI-3
A5ED-A43-1X4-MRI	80-001880RI-2	80-001880RI-3
A5ED-B44-1X4-MRI	80-001881RI-2	80-001881RI-3

See MitySOM-A5E Datasheet and Carrier Board Design Guide for migration options across the MitySOM-A5E family.

6 Document Revision History

Date	Version	Change Description
24-September-2026	1.0	Initial Version