MitySOM-A5E Development Kit Board
80-001828RI

Revision History and Errata

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1 Introduction

This document describes the production revision history for any known design issues or exceptions to the functional specifications for the MitySOM-A5E Standard Development Kit Carrier I/O Board developed by Critical Link LLC.

Details regarding the development kit carrier board may be accessed at https://www.criticallink.com/product/mitysom-a5e-standard-dev-kit/, and additional support information may be located at https://support.criticallink.com/redmine/projects/mitysom_a5/wiki.

This document is subject to change without notification. However, the most recent version of this document will be made available at the website mentioned above. The website supports email notification (via the “watch option”) for changes to documents published.

2 Product Marking

The board serial number may be visually read from a label affixed to the board. The board Printed Circuit Assembly (PCA) number may also be visually read from a label affixed to the board. The Printed Circuit Board (PCB) part number and revision are etched in copper, also visible on the board.

The serial number is of the format “S/NXXXXXX”, where XXXXXX is the serial number. The PCA part number begins with “80-“. The PCB revision begins with a “90-“.

3 PCA Product History

The PCA product history for all MitySOM-A5E Standard Development Kit boards is listed below. Details for Product Change Notifications (PCNs) may be downloaded from the link below.

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Errata_and_Module_Product_Change_Notifications

Table 1 highlights the PCA product history for all MitySOM-A5E Standard Development Kit Boards.

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Table 1 PCA Product History

PCA Number	Applicable Design Exceptions	PCNs
80-001828RI-4*	4.1 High Insertion/Return Loss of SFP28 Cage above 17G 4.2 Support needed for additional MIPI camera interfaces 4.3 AC Coupling Capacitors Incorrect value 4.4 UHS modes requiring 1.8V IO voltage on microSD card not supported 4.5 Mounting holes for m.2 connectors too large 4.6 Main Clock PLL Not Programmed on Power Up 4.7 Cannot configure RS1 pin on SFP28 Media converters 4.8 Cannot control I2C_EMAC0 (MIPI camera I2C buses) with FPGA pins 4.9 Strong Pullup Required on I3C0 SDA 4.10 No AC Coupling Capacitors on FMC GBTCLK0/1_M2C clock lines 4.11 PCIe Reset Connections for RP devices do not follow Altera Guidelines	
80-001828RI-7	4.10 No AC Coupling Capacitors on FMC GBTCLK0/1_M2C clock lines 4.11 PCIe Reset Connections for RP devices do not follow Altera Guidelines 4.12 Pullup Resistors missing on RS1 level translators SFP28 connectors	PCN20261016000

*Early adopters having boards with revisions marked with -1, -2, or -3 should contact Critical Link for details regarding modifications applied to the hardware. Revisions -5 and -6 were internal engineering builds and were not shipped.

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4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to the baseline specification for the MitySOM-A5E Development Kit Carrier Board.

4.1 High Insertion/Return Loss of SFP28 Cage above 17G

Issue Description

Above 17G, the insertion and return loss of transceiver data lanes going to both SFP28 cage connectors exceeds design margins.

Design Impact

Operation of the SFP28 cage with MitySOM-A5E SOMs with Group A Agilex 5 devices at 25 Gbps may result in higher-than-expected bit error rates (BER).

Planned Resolution

The layout of the transceiver lanes to the SFP28 cages, as well as the PCIe devices and the FMC interface connector, has been updated to reduce insertion and return loss to within design margin, supporting proper 25 Gbps throughput.

This issue is addressed in PCN20261016000.

4.2 Support needed for additional MIPI camera interfaces

Issue Description

The initial design of the carrier card provided support for up to 5 MIPI camera interfaces. There has been demand for additional MIPI camera support.

Design Impact

Only 5 MIPI cameras are supported in the original design.

Planned Resolution

Three additional MIPI camera interfaces have been added to the carrier card design leveraging unused HSIO interface pins, allowing up to 8 MIPI cameras to be utilized.

This issue is addressed in PCN20261016000.

4.3 AC Coupling Capacitors Incorrect value

Issue Description

The initial design of the carrier card utilized 100 nF AC coupling capacitors on the transceiver transmit data lanes for all the PCIe express interfaces (m.2 E-Key, m.2 M-Key, and PCIe edge connector). The 100 nF AC coupling capacitor value is valid only for PCIe Gen 2 and 1. The PCIe CEM specifications call for a

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nominal 220 nF AC coupling capacitance due to the potential DC imbalance of the symbol coding.

Design Impact
Operation of the PCIe links above 5 Gbps (Gen 2 speeds) may exhibit higher than expected bit error rate (BER).

Planned Resolution
The capacitors have been updated to use 220 nF devices.

This issue is addressed in PCN20261016000.

4.4 UHS modes requiring 1.8V IO voltage on microSD card not supported

Issue Description
The initial design of the carrier card utilized a simple 1.8V to 3.3V level translator to interface with the microSD card. This required the IO voltage on the microSD card to be held at 3.3V, and High-Speed UHS modes were not supported.

Design Impact
The maximum read and write throughput was limited to 50 MHz (burst of 25 MB/s).

Planned Resolution
The design has been updated to support Voltage switching using an HPS GPIO pin to control the desired IO voltage level (default 3.3V, 1.8V selectable). This allows the microSD card to be operated using High-Speed UHS modes (SDR50, SDR104, DDR50).

This issue is addressed in PCN20261016000.

4.5 Mounting holes for m.2 connectors too large

Issue Description
The initial design of the carrier card used hole sizes that were too large for the intended PEM mounting hardware suitable for fastening inserted m.2 cards into the slots.

Design Impact
Non-standard mounting hardware was necessary to secure installed m.2 cards in the system.

Planned Resolution
The design has been updated to support the proper mounting hardware. On the m.2 M key interface, the mounting hardware for the 80 mm slot length cards has been fitted.

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This issue is addressed in PCN20261016000.

4.6 Main Clock PLL Not Programmed on Power Up

Issue Description
U68, the Si5332A PLL chip providing reference clocks for all of the Agilex 5 transceivers except the PCIe EP device, is not configured / programmed after power up. None of the reference clocks are available immediately after power on.

Design Impact
The current reference designs include a uBoot based script that will program the PLL chip via the HPS I2C1 interface. Details regarding this programming procedure and configuration of the clock outputs are included on the following support site web page:

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Programming_the_DevKit_Silicon_Labs_PLL

This requires developers to instantiate an HPS into their design and configure it to load and run the uBoot software (or their own custom software) to program the PLL clock device. This can be an issue for customers utilizing the SOM without wanting to use / configure the HPS.

Planned Resolution
The design has been updated to preprogram the U68 SI5332A PLL chip with the frequency plan mentioned in the above link on the support site. This will allow leveraging the standard transceiver interfaces without the need to program the chip on power up.

This issue is addressed in PCN20261016000.

4.7 Cannot configure RS1 pin on SFP28 Media converters

Issue Description
The initial design of the carrier card tied pin 9 of the SFP28 cage connectors (J5 and J6) to ground. Pin 9 is the rate select 1 (RS1) pin on SFP28 media converters, and should be controllable to select between 10 Gbps and 25 Gbps data rates.

Design Impact
It was not possible to strap the RS1 pin high to select 25 Gbps data rates on installed SFP28 media converters.

Planned Resolution

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The design has been updated to provide two FPGA pins to control the RS1 pin of both SFP28 interfaces. These pins should be driven low when SFP or SFP+ (10 Gbps and below) modules are installed.

This issue is addressed in PCN20261016000.

4.8 Cannot control I2C_EMAC0 (MIPI camera I2C buses) with FPGA pins

Issue Description
The initial design of the carrier card attached the I2C bus signals for all the MIPI camera interfaces to HPS I2C_EMAC0, which can only be accessed by the HPS subsystem.

Design Impact
It was not possible to send commands to the MIPI camera I2C interfaces with an FPGA fabric only design.

Planned Resolution
The design has been updated to provide the capability to override the HPS I2C_EMAC0 pins using FPGA HSIO pins and an enable switch.

This issue is addressed in PCN20261016000.

4.9 Strong Pullup Required on I3C0 SDA

Issue Description
To support multiple I3C devices on the I3C0 bus, a strong pullup (1K) must be dynamically enabled on the SDA line during bus mastering operation. The initial design did not include provisions for this capability.

Design Impact
Signal Integrity on the I3C0 expansion bus was marginal when driving multiple devices.

Planned Resolution
The design has been updated to provide the capability to dynamically enable a 1K strong pullup resistor on the SDA line using the HPS I3C0_SDA_PULLUP_EN signal.

This issue is addressed in PCN20261016000.

4.10 No AC Coupling Capacitors on FMC GBTCLK0/1_M2C clock lines

Issue Description

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The carrier card routes the FMC GBTCLK0_M2C and GBTCLK1_M2C differential clocks directly from the FMC carrier card to the MitySOM-A5E Agilex 5 transceiver clock input pins. The FMC specification calls for these clocks to be LVDS. The Agilex 5 does not support direct connection to LVDS clocks, they must be AC coupled to bring the common mode voltage within the clock input specification of the FPGA device.

Design Impact
Customers should not utilize FMC cards driving the GBTCLK0 or GBTCLK1 clock lanes using LVDS signaling if they are not AC coupled on the mezzanine card.

Planned Resolution
Critical Link is assessing how to resolve this issue. On the next board update, AC coupling capacitors will be added. Contact Critical Link if you have issues with routing FMC clocks to the Agilex 5 FPGA to see if a work-around can be provided.

4.11 PCIe Reset Connections for RP devices do not follow Altera Guidelines

Issue Description
For the PCIe Root Port (RP) devices (m.2 M-Key and m.2 E-Key), the Agilex 5 HIP hardwired perst_n signal is connected to the PCIe PERSTN interface pin as shown in Figure 1.

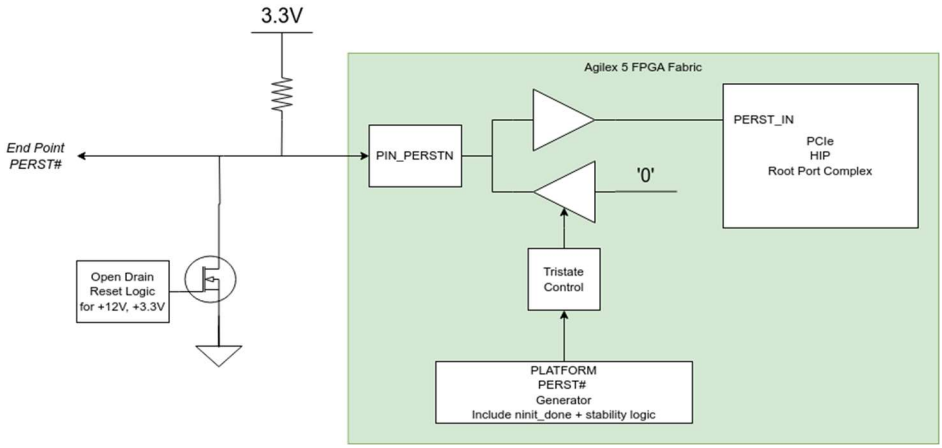


Figure 1 Current PCIe Root Port Implementation on m.2 Connectors

This is not the intended connection recommended by the Altera PCIe IP design team. In RP mode, the proper connection should be to drive the hardwired perst_n signal in the HVIO pin with a signal that indicates the reference clock is present and the fabric HIP controller should be taken out of reset, while using a separate HVIO (GPIO) pin to drive the PCIe PERSTN interface pin independently from the HIP reset pin. This is illustrated in Figure 2.

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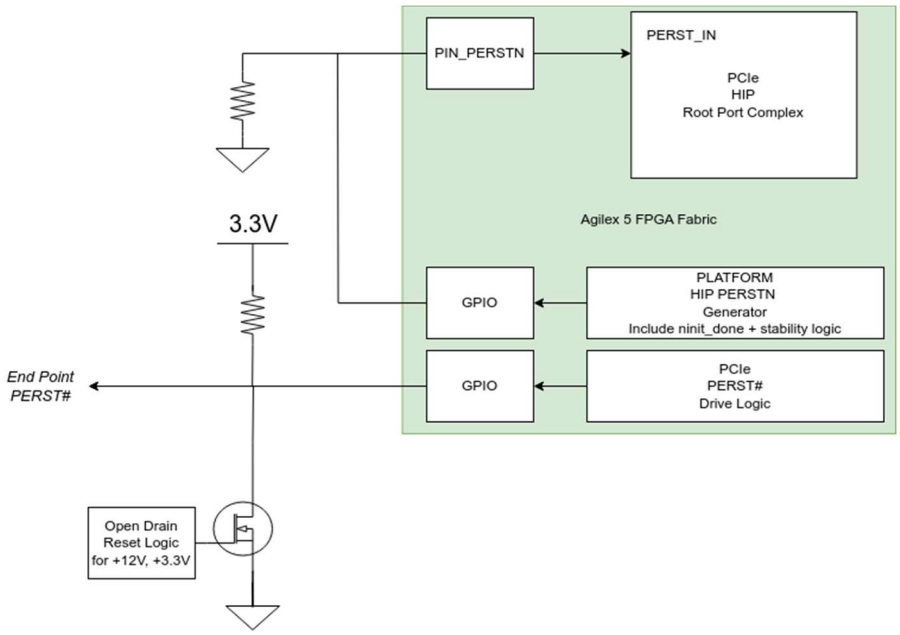


Figure 2 Altera Intended Reset Implementation for RP Connections

Design Impact

With the existing design, both the HIP and the external EP card will be reset simultaneously when the signal is driven by the external monitoring circuitry or by the FPGA, which can be accomplished by defining the perst_n signal as an IO pin and using the following style logic:

perst_n <= ‘0’ when drive_reset=’1’ else ‘Z’;

It is not possible to reset the external EP card without resetting the local HIP.

Planned Resolution

Critical Link is assessing how to resolve this issue on the next board update. If this issue is blocking development, please contact Critical Link for rework options or other potential work-arounds.

4.12 Pullup Resistors missing on RS1 level translators SFP28 connectors

Issue Description

Revision -7 carrier cards utilize an LSF0102DCTR to translate a 1.3V FPGA HSIO control signal to a 3.3V control signal for the RS1 signals (pin 9) of each of the two SFP28 module interface connectors. The design is missing a pullup resistor on the +3.3V side of the LSF0102DCTR device. This results in a +1.3V signal applied on the +3.3V side of the translator when a high is selected instead of the intended +3.3V level.

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Design Impact
Customers should avoid using media converters requiring a valid RS1 signal that has a V_{IL} that exceeds 1.3V. Contact Critical Link for rework options if an RS1 signal above 1.3V is required.

Planned Resolution
The pullup resistors will be added on the next release of the board to properly drive RS1 to +3.3V when commanded.

5 REVISION HISTORY

Date	Version	Change Description
16-OCT-2026	1.0	Initial release

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