MitySOM-5CSX System-On-Module (SOM)

Revision History and Errata

1 Introduction

This document describes the production revision history and any known design issues or exceptions to the functional specifications for the MitySOM-5CSX Module developed by Critical Link, LLC. For the purposes of this document, reference to the "module" implies MitySOM-5CSX System-On-Module.

Details regarding the board may be accessed at http://www.criticallink.com/product/mitysom-5csx/, and additional support information is located at the following URL: http://redmine.syr.criticallink.com/redmine/projects/mityarm-5cs/wiki. This document is subject to change without notification. However, the most recent version of this document will be made available at the website mentioned above. The website supports email notification (via the "watch option") for changes to published documents.

2 Product Marking

The board's PCA number and serial number may be visually read from a label affixed to the bottom of the module. The Printed Circuit Board (PCB) part number and revision is etched in copper, also visible on the bottom.

The PCA number begins with "80-". The PCA number can also be determined by the serial number, if necessary. Contact Critical Link for details.

The serial number is of the format "S/NXXXXXX", where XXXXXX is the serial number.

The PCB part number begins with "90-".

3 PCA Product History

The PCA product history for all MitySOM-5CSX SOMs is listed in Table 1. Details for Product Change Notifications (PCNs) may be downloaded from the link below. Table 1 highlights the PCA product history for the MitySOM-5CSX module.

http://redmine.syr.criticallink.com/redmine/projects/mityarm-5cs/wiki/Errata_and_Module_Product_Change_Notifications

Table 1 Revision History

Model Number	PCA Number	Errata	PCN
5CSX-H6-42A-RC-X	80-000569RC-2 80-000620RC-2	4.1.1 Early Silicon Cyclone V Device 4.2.1 Pre-production Power Supply Device 4.3.1 QSPI Read Errors at 50MHz and Higher 4.4.1 FPGA DDR3 Requires Chip Select 4.5.1 I2C LED Controller Connections	
5CSX-H6-42A-RC 5CSX-H6-42A-RI 5CSX-H6-53B-RC 5CSX-H6-53B-RI 5CSE-S2-3XA-RC	80-000642RC-1 80-000642RI-1 80-000646RC-1 80-000646RI-1 80-000647RC-1		PCN20140513000

4 Known Design Exceptions and Usage Notes

This section outlines the design exceptions to MitySOM-5CSX module.

4.1 Cyclone V

4.1.1 Early Silicon Cyclone V Device

Issue Description

The Altera Cyclone V used on the initial MitySOM-5CSX modules is an Early Silicon (ES) device. To easily identify the modules with ES silicon parts, the power LED (D5) is orange instead of green.

Design Impact

The errata Altera has identified with the ES devices will exist for these initial modules. Please refer to Altera's documentation for further details:
http://www.altera.com/literature/es/es_cyclone_v.pdf

Planned Resolution

Production devices will be used on future modules. The modules with production parts on them will include a green power LED.

This is addressed by PCN 20140513000.

4.2 Power

4.2.1 Pre-production Power Supply Device

Issue Description

The initial MitySOM-5CSX modules include a Linear Tech power supply that is a pre-production device.

Design Impact

The LT8612 power supply is known to have switching edges that are faster than desired according to Linear Technology's evaluation of the part. This may result in higher radiated and conducted emissions than the final modules will exhibit.

Planned Resolution

Production devices will be used on future modules.

This is addressed by PCN 20140513000.

4.3 QuadSPI NOR Flash

4.3.1 QSPI Read Errors at 50MHz and Higher

Issue Description

The QSPI interface experiences read errors when running at 50MHz or higher. The QSPI interface is able to write reliably, but read tests exhibit errors. Critical Link, LLC is investigating this issue.

Design Impact

Booting the HPS from QSPI NOR Flash does not currently work when set to the fast CSEL option.

Workaround

To boot the HPS from the QSPI NOR Flash, set the CSEL mode to "00". The preloader must also be generated to run the QSPI interface at the slower rate, around 10MHz.

Planned Resolution

This is addressed by PCN 20140513000.

4.4 FPGA DDR3 Interface

4.4.1 FPGA DDR3 Requires Chip Select

Issue Description

The FPGA DDR3 interface connected to Banks 3A, 5A, and 5B does not include a connection to the chip select. According to Micron data sheets, the chip select is not required to run a single DDR3 SDRAM and it can be simply tied active. However, the Altera memory controller does require a chip select connection for advancing through the memory DDR3 modes.

With the DDR3 chip select tied active, the FPGA DDR3 interface fails to complete calibration and the DDR3 memory cannot be used with the UniPHY controller. Once the chip select line is connected, the FPGA DDR3 interface successfully completes calibration and is fully functional.

Design Impact 80-000569RC-2

This module does not support the UniPHY DDR3 memory controller and there is presently no alternate controller identified that will work.

Design Impact 80-000620RC-1

This module has an additional jumper installed from pin 21 of the edge connector to the FPGA DDR3 Chip Select (CS) pin. When this is used in the FPGA design as the FPGA DDR3 CS pin, the FPGA DDR3 SDRAM is able to complete calibration and function properly.

The edge connector pin 21 is exposed to support the PCI Express reset connection (B5A–PERSTL1–N) or a general FPGA I/O connection. External connections to this pin cannot be used without impacting the functionality of the SDRAM chip select.

WARNING: The jumper installed on this module to support the chip select is a fragile connection. The jumper connection is made to the very end of the edge connector's finger and could be broken free easily. Handle this module with care.

Planned Resolution

The future module revisions will include the FPGA DDR3 chip select connection without consuming the B5A–PERSTL1–N connection to the edge connector. This will allow the designs to fully take advantage of both the PCI Express interface and the FPGA DDR3 chip on the module.

This is addressed by PCN 20140513000.

4.5 I²C Interface

4.5.1 I²C LED Controller Connections

Issue Description

The LED color connections inhibit the intended software control.

Design Impact
Future modules will change the order of connections to the various colors. Once the color assignments are reordered, the controller's color cycling feature will be supported. The AUX is an orange LED to indicate ES device is on the module. Once the modules are built with production silicon, the AUX LED will be green.

Workaround

Software controls these outputs and can drive the LEDs to generate the desired color output.

Planned Resolution

The full production modules will connect the LEDs in the order of red, green, blue, and an auxiliary green LED for easier software control. Refer to Table 2 for color assignment details.

This is addressed by PCN 20140513000.
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Table 2: I²C LED Colors

Output	Initial	Desired
CURR1(B2)	green	red
CURR2(C1)	aux (orange)	green
CURR3(A1)	red	blue
CURR4(D1)	blue	aux (green)

5 REVISION HISTORY

Date	Version	Change Description
01-Oct-2013	1.0	Initial Release
13-May-2014	1.1	Add PCN 20140513000 information. Update Title and wiki links.
09-Jan-2015	1.2	Corrected Table 1.
12-Dec-2015	1.3	Corrected Title to reflect errata is for engineering silicon processor (5CSX-x) designs. Separate errata being released for production silicon (5CSx) designs.