PCN# 20261016000

Improve transceiver margins above 17G, add additional MIPI cameras, update m.2 mounting hardware, update PCIe AC coupling capacitors, pre-program U68 PLL, support UHS 1.8V modes on microSD card, allow FPGA fabric to override I2C_EMAC0, support SFP28 RS1 signals, and provide I3C0 strong pullup control on the

MitySOM-A5E
Development Kit Carrier Card

Date: October 16, 2026

To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact info@criticallink.com

Sincerely,

Critical Link, LLC

Phone: (315) 425-4045

Fax: (315) 425-4048

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PCN Number: 20261016000

PCN Date: October 16, 2026

Title: Improve transceiver margins above 17G, add additional MIPI cameras, update m.2 mounting hardware, update PCIe AC coupling capacitors, pre-program U68 PLL, support UHS 1.8V modes on microSD card, allow FPGA fabric to override I2C_EMAC0, support SFP28 RS1 signals, and provide I3C0 strong pullup control

Contact: info@criticallink.com

Phone: (315) 425-4045

Ship Date: Starting October 2026

Overview

Changes to MitySOM-A5E Development Kit Carrier Card are identified in the following sections.

1 Improve Transceiver Margins above 17G

1.1 Description of Change

The trace layout of the GTS transceivers between the MitySOM-A5E connectors and the SFP28 cages, the m.2 M Key slot, the m.2 E Key slot, the FMC connector, and the PCIe Edge interface has been optimized to improve signal integrity margins, particularly for the SFP28 signals that may operate above 17G. This has been accomplished by refining the signal via anti-pads and ground return vias.

1.2 Reason for Change

To support operating the carrier card SFP28 links with Group A Agilex-5 devices at 25 Gbps, the trace routing has been enhanced to provide acceptable signal integrity margins.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

This change should not affect form or fit. With this change, operating the SFP28 links above 17G (device Group A speeds) will work with acceptable bit error rates (BER).

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

None.

2 Add additional MIPI cameras

2.1 Description of Change

Three additional MIPI camera interface connectors (J24, J25, J26 – bottom side of board) have been added and connected to spare/unused HSIO pins on the MitySOM-A5E connector interface. The MIPI interface signals added are described in the table below.

Table 1 Additional Pins related to the 3 new MIPI Cameras

SOM Pin	FPGA Pin	Previous Function	New Function
J2-C28	CK66	No Connection	CSI8_RX0_P

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SOM Pin	FPGA Pin	Previous Function	New Function
J2-C27	CL70	No Connection	CSI8_RX0_N
J2-F27	CK73	No Connection	CSI8_RX1_P
J2-F28	CL73	No Connection	CSI8_RX1_N
J2-A30	CK63	No Connection	CSI8_RXCLK_P
J2-A29	CL66	No Connection	CSI8_RXCLK_N
J2-C31	CL56	No Connection	CSI8_RX2_P
J2-C30	CL60	No Connection	CSI8_RX2_N
J2-F31	CK56	No Connection	CSI8_RX3_P
J2-F32	CL54	No Connection	CSI8_RX3_N
J2-F34	CL42	No Connection	CSI7_RX0_P
J2-F33	CK45	No Connection	CSI7_RX0_N
J2-C33	CK48	No Connection	CSI7_RX1_P
J2-C34	CL45	No Connection	CSI7_RX1_N
J2-C36	CK39	No Connection	CSI7_RXCLK_P
J2-C37	CL39	No Connection	CSI7_RXCLK_N
J2-G35	CK35	No Connection	CSI7_RX2_P
J2-G34	CL35	No Connection	CSI7_RX2_N
J2-F36	CK33	No Connection	CSI7_RX3_P
J2-F37	CL30	No Connection	CSI7_RX3_N
J2-E27	CF52	No Connection	CSI6_RX0_P
J2-E28	CH52	No Connection	CSI6_RX0_N
J2-D27	CC52	No Connection	CSI6_RX1_P
J2-D26	CA52	No Connection	CSI6_RX1_N
J2-E29	CF49	No Connection	CSI6_RXCLK_P
J2-E30	CH49	No Connection	CSI6_RXCLK_N
J2-E33	CH41	No Connection	CSI6_RX2_P
J2-E32	CF41	No Connection	CSI6_RX2_N
J2-D30	CC41	No Connection	CSI6_RX3_P
J2-D29	CA41	No Connection	CSI6_RX3_N

The CAM6, CAM7, and CAM8 control SCL/SDA lines have been added to the previously unused bus 5, 6, and 7 of the U43 I2C Mux expansion circuit. To control the 2 GPIO lines on each camera, U74, a PCAL6408APWJ I2C IO expander was added on the CAM6 I2C port (bus 5 of the mux expansion bus) at address 0x21 with the following IO assignments:

Table 2 Additional MIPI Camera GPIO pin routing to I2C Expander

U74 Port Expander GPIO Port	Function
P0	CAM6_IO1
P1	CAM6_IO2
P2	CAM7_IO1
P3	CAM7_IO2
P4	CAM8_IO1
P5	CAM8_IO2

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2.2 Reason for Change

Customer demand for additional MIPI cameras drove the decision to include the additional connectors.

2.3 Anticipated Impact on Form, Fit, Function

There is no impact to form. The location of the existing connectors on the design has not changed. The additional 3 connectors are located on the bottom of the board. They are low profile flat-flex connectors, they will not interfere with any existing mounting hardware that may be used. The camera interfaces use previously unassigned pins on the board. No impact is expected to existing FPGA designs.

2.4 Anticipated Impact on Quality or Reliability

None.

3 Update m.2 mounting hardware

3.1 Description of Change

The mounting holes for the m.2 E-key and M-Key were updated to support installation of SM3ZS067U410-NUT1-R1200. This is a standoff providing the correct height and mounting thread for a standard m.2 card installation. For the M-Key slot, the 80mm mounting hole includes the standoff.

3.2 Reason for Change

The mounting holes used in the initial design require use of non-standard mounting hardware for m.2 devices.

3.3 Anticipated Impact on Form, Fit, Function

There is no impact to form or function. For fit, standard 2.5mm mounting hardware may be used to install M-Key or E-Key cards.

3.4 Anticipated Impact on Quality or Reliability

Installed m.2 cards can be secured with standard mounting hardware. There is no adverse impact to quality or reliability.

4 Update PCIe AC coupling capacitors

4.1 Description of Change

The AC coupling capacitors for the transmit lanes on the PCIe Edge interface (C135, C136, C137, C138, C139, C140, C141, C142), the m.2 M-Key (C117, C118, C120, C121, C122, C125, C131, C132), and the m.2 E-Key (C133, C134) interfaces were changed from 100 nF to 220 nF.

4.2 Reason for Change

The change in capacitance brings the design into compliance with PCIe Gen 3 and higher CEM requirements.

4.3 Anticipated Impact on Form, Fit, Function

None.

4.4 Anticipated Impact on Quality or Reliability

When operating the PCIe interfaces at Gen 3 or Gen 4 speeds, it is expected that the bit error rate should be lower. There is no impact on reliability.

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5 Pre-Program U68 (Si5332A PLL)

5.1 Description of Change

The Si5332A Phase Lock Loop (PLL) clock generator device, reference designator U68, is now preprogrammed using the one time programmable (OTP) non-volatile memory (NVM) according to the frequency plan documented on the following Critical Link support page:

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Programming_the_DevKit_Silicon_Labs_PLL

5.2 Reason for Change

The change allows FPGA only designs to leverage the reference clocks provided by U68 without the need to instantiate the HPS and run software to program and enable the device via I2C.

5.3 Anticipated Impact on Form, Fit, Function

No change to form or fit. Functionally, users may modify the frequency plan via the I2C interface as before, but for typical interfaces that will work with the advertised frequency plan that step will no longer be required.

5.4 Anticipated Impact on Quality or Reliability

No impact.

6 Support UHS 1.8V modes on microSD card

6.1 Description of Change

U1, LSF0108PWR, a 1.8V to static 3.3V level converter interfacing to the HPS MMC/SDIO interface, has been replaced with U75, NVT4858HKZ, which supports 1.8V or 3.3V translation on the micro-SD connector side of the interface. A voltage select IC, U1 (FPF1320UCX), has been added to allow switching between 3.3V and 1.8V for the IO voltage rail on the micro-SD card signals. The following changes to the FPGA pin assignments related to this change are listed in Table 3. Customers migrating to revision -7 or later boards will need to update their software to move the location or disable the SGMII reset pin and enable the SD_VSEL_3V3 to leverage the higher speeds.

Table 3 SOM Connection Changes Related to 1.8V microSD card support

SOM Pin	FPGA Pin	Old Function	New Function
J1-F41	AG123	ETH2_RESETN (SGMII PHY Reset Pin)	SD_VSEL_3V3 (high=3.3V, low=1.8V)
J2-F12	CF92	No Connect	ETH2_RESETN

6.2 Reason for Change

The change supports operating the microSD card using higher speed UHS modes (SDR50, SDR104, DDR50).

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6.3 Anticipated Impact on Form, Fit, Function

No change to form or fit. Functionally, the microSD card can be configured to achieve higher throughput using the SD_VSEL_3V3 control pin and enabling the UHS modes in the linux kernel driver.

6.4 Anticipated Impact on Quality or Reliability

None.

7 Allow FPGA fabric to override I2C_EMAC0

7.1 Description of Change

Two FPGA HSIO Bank 2A pins have been conditionally connected to the I2C_EMAC0 bus via a level translator chip, U73, which can be enabled or disabled by switch S7. This allows the FPGA to optionally control and monitor the I2C_EMAC0 bus pins on the carrier card. The additional pins connected are shown in the table below.

Table 4 SOM Connection Changes Related to FPGA override of I2C_EMAC0

SOM Pin	FPGA Pin	Old Function	New Function
J2-H13	CL76	No Connect	I2C_EMAC0_SDA_OVERRIDE
J2-H12	CK76	No Connect	I2C_EMAC0_SCL_OVERRIDE

7.2 Reason for Change

The change supports operating the I2C_EMAC0 bus using an FPGA bitstream that does not require instantiation or use of the HPS / HPSIO connection.

7.3 Anticipated Impact on Form, Fit, Function

No change to form or fit. Functionally, if the S7 switch is disabled, there is no change. If the S7 switch is enabled, the HPS control of I2C_EMAC0 should be disabled and control of the bus should be managed through the pins noted in Table 4.

7.4 Anticipated Impact on Quality or Reliability

None.

8 Support driving Rate Select 1 (RS1) signals on SFP28 connectors

8.1 Description of Change

Two FPGA HSIO Bank 2A pins have been connected to pin 9 of each of the SFP28 edge connectors, J5 and J6, through level translator U77. The additional pins connected are shown in the table below. However, pullup resistors were not included on the +3.3V side of the RS1 level translator. Therefore, the maximum voltage applied on the RS1 signal is currently 1.3V. Customers should review the specifications for the media converters they intend to use to ensure they will function with this configuration. The pullups will be added in the next release of the board.

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Table 5 SOM Connection Changes Related to supporting control of RS1 Signals

SOM Pin	FPGA Pin (1.3V)	Old Function	New Function
J2-C13	CH81	No Connect	SFP1_RS1
J2-H09	CL82	No Connect	SFP2_RS1

8.2 Reason for Change

The change supports controlling the rate select mode for SFP28 capable media converters installed in the SFP28 cages. Previously this signal had been grounded and limited rate selection to lower frequencies.

8.3 Anticipated Impact on Form, Fit, Function

No change to form or fit. With this change, the 25 Gbps rate can be selected under FPGA control. When SFP or SFP+ connections are used, the Rate Select 1 pins should be driven low by the FPGA.

8.4 Anticipated Impact on Quality or Reliability

None.

9 Support optional strong SDA pullup I3C0 Expansion Bus

9.1 Description of Change

A single pole double throw switch, S6, was added to support using HPS GPIO1_20 as either the FAN_ENABLE signal or as the I3C0_SDA_PULLUP_EN signal. The I3C0_SDA_PULLUP_EN signal causes a strong (1k Ohm) resistor to be added to the pullup resistance on the I3C0_SDA signal on J21. When the FAN_ENABLE signal is selected, the I3C0_SDA_PULLUP circuit will default to a weak pullup state (20K). When the I3C0_SDA_PULLUP_EN signal is enabled, the FAN_ENABLE signal will default to low / disabled state.

Table 6 SOM Connection Changes Related to enabling strong pullup on I3C0 SDA

SOM Pin	FPGA Pin	Old Function	New Function
J1-E45	F127	FAN_ENABLE	FAN_ENABLE (S6=off) I3C0_SDA_PU_EN (S6=on)

9.2 Reason for Change

Customers requiring the strong pullup control for the I3C0 bus can now select this function and test the Agilex 5 I3C0 bus.

9.3 Anticipated Impact on Form, Fit, Function

No change to form or fit. With this change, customers should be able to integrate I3C0 high speed devices with J21.

9.4 Anticipated Impact on Quality or Reliability

None.

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10 Products Affected

Details regarding the full revision history are in the MitySOM-A5E Revision History and Errata on the Critical Link support site at the link below.

https://support.criticallink.com/redmine/projects/mitysom_a5/wiki/Errata_and_Module_Product_Change_Notifications

Table 7 Products Affected

Starting PCA	Replacement PCA
80-001828RI-4	80-001828RI-7

See MitySOM-A5E Datasheet and Carrier Board Design Guide for migration options across the MitySOM-A5E family.

11 Document Revision History

Date	Version	Change Description
16-October-2026	1.0	Initial Version

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